LMD 9200 Series TS1/TS2 Controller Operating Manual

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PEEK TRAFFIC SYSTEMS, INC.

LMD 9200 SERIES CONTROLLER OPERATING MANUAL

The information contained within this manual is intended to serve as a guide to users in the maintenance and operation of the LMD 9200 traffic signal controller. An effort has been made to ensure the accuracy of the information contained in this manual. However, the information is supplied without warranty of any kind. Further, there is no warranty of the applicability of the information to all cases. The user is cautioned to fully program and thoroughly test the controller for its intended application prior to placing it in operational service. PEEK Traffic Systems, Inc. reserves the right to add, delete, and/or modify the material in this manual at any time.

LMD9200 CONTROLLER UNIT

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SECTION I

LMD9000 SERIES GENERAL INFORMATION

GENERAL DESCRIPTION

The Traffic Control Technologies LMD9000 Series traffic controller unit is a 2-8 NEMA actuated controller using a MENU format for data entry. The unit provides traffic responsive signalized control of vehicles and pedestrians and is characterized by microprocessor control, keyboard data entry, a 40 column by 4 row back-lighted liquid crystal display, and a front fold-down panel for easy access.

The LMD Series controller can be programmed for either sequential or concurrent timing in various sequences from two phase semi actuated to eight phase fully actuated applications.

INTERFACE

The LMD9000 Series controller exceeds all requirements set forth in the NEMA (National Electrical Manufacturers Association) TS-1 or TS-2 type 1 and type 2 specifications.

The LMD9000 is capable of operating in any of three modes, including; TS-1, TS-2 type 2 and TS-2 type 1. The LMD9000 is available in two hardware configurations; The LMD9200 (type 2) which utilizes the industry standard MSA, MSB, and MSC connectors for back-panel interface, and the LMD9100 (type 1) which utilizes a serial communication link to interface with the backpanel, detector rack, and MMU (malfunction management unit). See I/O Section for more information on type 1 cabinet interface. It is the LMD9200 series controller which is also capable (downward compatible) of operating in the TS-1 mode, utilizing MSA, MSB, and MSC. All three versions share common features and functions , with the obvious exception of certain I/O (input/output functions).

INFORMATION MEMORY CARD

Timing and control data are entered into EEPROM (non-volatile memory) directly through the front panel keyboard. The EEPROM data as well as real time information are stored on a removable **Information Memory Card** (IMC) on the fold down panel. This card can be used to transfer data and the real time (time of day, date, year) from one unit to another without keystroke procedures.

SEQUENCES

Sequences include 2-8 phase, single ring, dual ring, combinations single and dual, and alternate sequences (lead/lag). The Lead/lag operation allows independent reversal of phase pairs 1 & 2, 3 & 4, 5 & 6, and 7 & 8. Selection can be on an on/off basis, by DC inputs, or automatically by TOD or by selection of certain cycle/split/ offset combinations (timing plans). In the Cycle/Split select mode, up to 10 pattern changes can be selected from a choice of 16 possible lead/lag patterns.

OVERLAPS and PHASES AS OVERLAPS

Overlap phases can be programmed through the keyboard or by a NEMA overlap card. Delay operation is provided with self timed O/L yellow & red. Protected/ permissive operation is provided via "overlap inhibit" programming. Phase output drivers can be also be programmed as overlaps (with delays if desired).

The available configurations are described as follows:

BASE MODEL - LMD90UVW-XYZ

U= Aux I/O	V= Comm module	W= Mode	X= Software	Y= I/O module	Z= Reserved
0 = None	0 = None	A = Actuated	1 = TS-1 TCT Comm	1 = No O/L card w/sliding lock	
1 = Std. MSD	1 = RS-232, FSK	P = Pre-timed	2 = TS-2 TCT Comm	2 = No O/L card w/latching blocks	
2 = Metal MSD	2 = 15 pin comm, Fiber		3 = TS-2 NEMA Comm	3 = O/L card w/sliding lock	
	3 = RS-485, FSK		4 = TS-2 MIST Comm	4 = O/L card w/latching blocks	
	4 = RS-485, Fiber		5 = Reserved		

General Features

- Conditional Service and re-service with programmable conditional service max time.
- Phases used 1-8 on or off.
- Pre-set timing plans for 2, 3, 4, 5, 6, or 8 phase operation.
- Remote MUTCD Flash by clock, input or FSK communications.
- Five section head control with yellow blanking and phase restrictions.
- Overlap output inhibit logic for blanking arrows
- Auto-max and max extend
- Service and max plans
- Added max red
- Advance Warning
- Extensive I/O (input/output) programmability
- Internal component level diagnostics

Actuation Features

- Phase assignable detectors with switching, stretch, delay and disconnect.
- Volume density with Last Car Passage, Automatic Min recall, No recall options.
- Detector diagnostics with “max fail recall”
- Detector memory on or off
- Vehicle Recall modes; extension, maximum, soft, or ped recall.
- Detector Simulation with volume, saturation level, and input pulse width.
- Simultaneous Gap Out mode on or off
- Dual Entry mode; off, on, or called by CNA or SYS

Pedestrian Features

- Flashing Don’t Walk through Ped Clear
- Flashing Walk
- Conditional ped service
- Flashing Don’t Walk through Yellow.
- Exclusive ped
- Dual Enhanced ped--barrier phase walk (e.g. ph 2) waits for other ring walk (e.g. ph 6) if it starts early.
- Overlapping peds
- “Not ped” overlaps (O/L inhibited when selected ped active, often used for right turn O/L’s)
- Walk Rest Modifier (WRM)
- Alternate ped timing by time clock (TOD)

Reporting Features

- Calls up to 2 phone numbers
- Scheduled time of day call-ins
- Prioritized messages (alarms)
- Detector volume logging
- MOE’s (Measure of Effectiveness) with Computed speed and true speed, green utilization, volume, occupancy and more.
- User defined messages
- Conflict monitor (MMU) messages

Pre-emption Features

- 6 high and low priority pre-empt inputs
- Assignable priorities
- Special Intervals
- Coordination during pre-emption
- Per overlap Inhibits during pre-emption
- Memory on/off
- Flash override
- Delay before pre-emption
- Omit non pre-empt phases and all peds during “last x” seconds of delay
- Minimum re-service
- Priority return option to return to interrupted phase(s)
- Hold only pre-emption
- Flashing Don’t Walk through yellow during pre-emption.

Transit Priority General Features

- 6 TP inputs for “soft” form of prioritized service to transit vehicles.
- TP phases can extend settable amount past normal force off or max.
- Non-TP phases can be shortened to get to TP phase
- Unit offset seeks to compensate for TP phase extended timing.
- Control timing adjustment provided for customized control

Time Clock Features

With an internal clock standard in all units, the LMD can operate in response to time of day commands based on a yearly program. This function can be used to implement various modes of operation such as night time flash, and in conjunction with other controllers, wireless time based coordination. In this mode, each controller time clock simultaneously issues coordination commands.

The time clock battery back-up feature allows the clock to continue to keep time without power supplied, so there is no need to reprogram, or re-setup the time clock after power failure.

The clock is programmable by date & year. with:

- 99 year calendar
- 30 day (minimum) down-time clock
- Daylight savings time automatically adjusted (on/off)
- 4 sync reference modes
- 200 day program events (a change in CSO = 1 event)
- 15 day programs
- 10 week programs
- 35 exception days, repeat by date or by DOW, WOM, MOY (such as Memorial Day, the last Monday in May).

Time clock controlled functions

The LMD provides a number of functions which can be internally controlled by time of day (no wiring), as follows:

- Cycle, Split, Offset (timing plan)
- Flash
- Auxiliary MSD CKT's 1-4
- Call for system
- Call to Max II (both rings)
- Inhibit Max ring 1/2
- Call to Non Act I/II
- Min Recall all phases
- Vehicle call 1-8
- Ped call 1-8
- Vehicle omit 1-8
- Ped omit 1-8
- Conditional service and re-service (enable)
- Simultaneous Gap-Out (inhibit)
- Interconnect inhibit
- Sync Inhibit (offset outputs)
- Walk Rest Modifier (enable)
- Dual Entry (enable)
- Red Rest Mode ring 1/2 (enable)
- Omit Red Clearance ring 1/2
- Ped Recycle ring 1/2 (enable)
- Detector Low threshold Inhibit
- Det (continuous) Presence Inhibit
- Pre-empt call 1-6
- Max Plans 1-8
- Service Plans 1-8
- Alternate sequences (lag phases 1, 3, 5, 7)
- Inhibit Volume Density phase 1-8
- Exclusive ped (enable)
- Adaptive Split Control (enable)
- Inhibit overlaps A, B, C, D (stay in red)
- Enable schedule A telephone 1/2
- Enable schedule B telephone 1/2
- Enable schedule C telephone 1/2
- Inhibit detectors
- Alternate volume sampling period (enable)
- Volume data call-in/ collection enables
- Enable MOEs and alt. sample period
- Inhibit conditional ped
- Inhibit detector delay
- Call to free
- Dual Enhanced Ped enable
- Inhibit 5 section head control
- Call to time clock mode
- Increase Yellow & Red (by a settable percentage)
- Dimming (enable)
- Call to week program 10 (download from remote PC)

Coordination features

- Subordinated coordination mode
- Adaptive Split control
- Auto calculation of force-offs and permissives
- 8 cycles (TS-1)
- 4 splits/cycle (TS-1)
- 5 offsets/cycle (TS-1)

  or
- 32 Timing plans (TS-2)
- 5 offsets per timing plan (TS-2)

- 8 phase assignable force offs
- 8 phase assignable permissives
- Coordinated phases assigned per cycle/split combination
- Service/Max plans assigned per cycle/split combination
- Ped permissives auto-calculated from veh permissives
- Shortway/dwell/interrupter offset seeking

TIMING RANGES

Min Green	0-9.9 or 127 secs
Passage	0-9.9 or 127 secs
Yellow	3-9.9 or 127 secs
Red	0-9.9 or 127 secs
Max Timing	0-255 secs
Walk	0-9.9 or 127 secs
Ped Clearance	0-9.9 or 127 secs
Secs/Act, TBR, TTR, Min Gap	0-9.9 or 127 secs
Max Variable Initial	0-9.9 or 127 secs
Max Extension	0-9.9 or 127 secs
Auto Max	0-255 secs
Added Max Red	0-9.9 or 127 secs
Controller Min Flash	0-9.9 or 127 secs
First All Red After Flash	0-9.9 or 127 secs
Conditional Service Max Time	0-9.9 or 127 secs
Red Revert	0-9.9 or 127 secs
Cycle, Offsets, Dwell	0-255 secs
Split	0-255 secs, or 0-99% of cycle
Force offs, Perms, Ped Perms	0-255 secs
Pre-empt Intervals	0-9.9 or 127 secs
Pre-empt hold only time	0-9.9 or 127 secs
Delay Before Pre-empt	0-255 secs
Pre-empt last X veh, ped omit	0-9.9 or 127 secs
Det stretch/disconnect timing	0-9.9 or 127 secs
Pre-empt Minimum Re-service	0-99 minutes
Detector delay	0-9.9 or 127 secs
Detector extension	0-25.5 or 255 secs
Detector Fail Sampling Period	0-255 minutes
Detector Fail Under/Over Thresh	0-999 counts
Transit Priority Min Re-service	0-255 mins
Transit Priority Group Walk time	0-9.9 or 127 secs
All other Transit Priority timers	0-255 secs

DISPLAYS AND KEYBOARD

The LMD display operates in a true menu format whereby the display lists, in English, various categories from which the user may select. The base menu lists the most general category choices such program mode and run mode data. From this base menu, when a category is selected, a sub-menu appears listing further choices such as security code, controller, coordination, time clock, pre-emption, etc. Each sub-menu further breaks down the choices into more specific categories until the specific sections of data can be obtained. The display operates such that a user familiar with traffic terminology, but unfamiliar with the display can successfully operate the display by following menu selections.

Context sensitive help screens are provided, giving a description of the functions on each screen.

SECURITY CODE

An optional security code can be programmed, which when activated, allows data changes. The code automatically deactivates 10 minutes after the last user keystroke. With knowledge of the old security code, the security code can be changed or inhibited. The security code can be keyboard disabled (no code required for data entry).

RUN MODE INDICATIONS

The run or observation mode is used to display operational status of the unit. The **LMD** displays the following information upon user request:

Basic Timing Display

- Indicates G,Y,R,W, DW, TØN, Veh and Ped Act per phase
- Indicates G,Y,R per each overlap
- Indicates service plan in effect (0= none)
- Indicates current timing per ring of min gm, psg, max I/II, max plan timing, walk, don't walk, yellow, red
- Indicates if phase Is extending, has recall, or CNA
- Indicates termination mode: force off, max, gap-out
- Indicates if phase is in red or green rest state
- Indicates if phase is in conditional service or SGO mode
- Indicates if phase has hold applied, If ring has Inhibit max applied, or if unit has stop time or MCE applied
- Indicates if Gap is reducing, or variable initial is in effect
- Indicates Current timing of active cycle and offset
- Indicates active pre-empt
- Indicates active Transit Priority, TP phases and special timings

Coordination Timing Display

- Indicates local/master cycle and offset timers
- Indicates status of force offs and permissives 1-8
- Indicates Ped Permissive and Coord Hold Status
- Indicates, if TBC mode, current time of day

Coordination Mode Status Display

- Indicates active and selection mode of timing plan and C/S/O.
- Indicates coordination sync status, In or not in sync
- Indicates the cycle and offset in effect and their values
- Indicates the sync reference mode (if applicable)
- Indicates if unit is in system or free and why (in English).

Volume Density Status Display

- Indicates active phase(s) and max timer(s)
- Indicates if in variable initial and timer(s)
- Indicates TBR, TTR, PSG timers
- Indicates the current gap level(s)

Time Clock Display

- Indicates current time, date, week, year, day of week
- Indicates week and day program in effect
- indicates current clock selected service/max plan
- Indicates coordination mode, CLK, Manual, Int, Comm
- Indicates status of circuits

Input Status Display

- Indicates on/off status of all inputs
- Indicates if veh/ped calls are stored in memory

Phase Output Display

- Indicates status of R,Y,G,W,DW,TØN per phase outputs
- Indicates status of all remaining phase and O/L outputs

Per Ring Input Status Display

- Indicates status of all per ring inputs

Per Unit Status Display

- Indicates status of per unit inputs and outputs

Coded Status Bit Display

- Indicates coded status bits and interval

Phase Service Display

- Indicates the method of service of each phase, i.e. Max Recall, CNA, Detector Actuated, Max Fail recall, etc.

Pre-emption Status Displays

- Indicates status of pre-emption, sequence steps, pre-empt timing, delay before pre-empt, min re-service.

Comm Status Displays

- Indicates status of Comm Module I/O, Last call-in, and data Xfer information

Coordination modes

Time based coordination--Standard in all units. The LMD controller unit is capable of coordinated operation in response to internally generated time clock commands selecting cycle, split, and offset. In this mode the LMD is able to coordinate with other time base units without need of interconnect. Four sync reference modes are provided including; End of previous cycle, 8 independent (daily), absolute (one time), and event.

Hardwired Interconnect based coordination--requires optional MSD connector and board. Responds to traditional AC hardwire interconnect commands. The LMD can also drive an interconnect as a master without modification to the basic unit.

FSK Communications based coordination.--Requires optional modem connector & board (standard in TS-2 configuration). Allows full duplex communications with a closed loop system master or other central communications system.

Fiber-optic communications based coordination.--Requires optional internal or external modem. Allows full duplex communications with a closed loop system master or other central communications system.

Controller Components

The LMD9000 controller unit consists of a chassis capable of accepting a CPU board, a power supply board, one of two I/O boards, an AUX I/O (MSD) board, and a communications module.

The Control board directs and controls the operation of all other boards. The Z280 CPU, RAM, clock, Data EEPROM and operating Program PROMs are all located on the CPU board. The CPU is isolated from direct interface with the external environment.

The TS-2 type 2 I/O board (with MSA, MSB, and MSC) contains the load switch drivers for signal indication control. These drivers include the GREEN-YELLOW-RED-WALK-PED CLEARANCE-DON"T WALK outputs for the phase. Each driver output is at GROUND when TRUE and pulled up through a 10 K resistor to + 24 volts when FALSE. Thus, the complete controller assembly must include the necessary solid-state load switches as a separate entity from the controller unit which becomes the timing and sequencing device for control of the load switches.

The MSA, B, and C pin terminations are in conformance to the NEMA Standards. Included are the various input modifiers of controller unit operation–some of which are provided on a "per phase" basis while others are provided on a "per ring" or "per unit" basis.

The TS-2 type 2 I/O board contains only an MSA (19 pin) to provide the controller with 110 volts AC. Interface with the back-panel is made through a 15 pin RS-485 connector on the comm module utilizing an SDLC (synchronous data link communication) protocol.

The Aux I/O controls MSD I/O, such as time clock functions, interconnect functions (110 VAC), auxiliary functions (including phase detectors), pre-emption, etc.

RS232 PORT

An RS232-C industry standard I/O port is provided in all LMD units serving a variety of functions, including:

Unit to unit data transfer

Print-out of program data (interfaces with most standard serial printers)

Direct interface with desk-top personal or lap-top computer for upload/download of program data, etc.

Direct interface with a dial-up modem for communications over phone lines with a PC (no system master).

COMM MODULE

The LMD is expandable by addition of a module/board with connectors to provide remote communications. The communications provides a TDM FSK communications modem port, additional system I/O, and an additional RS-232 port. When inserted, the LMD unit is capable of full duplex FSK 1200 baud data transmission over a 4 wire 3002 voice grade link. The unit would typically communicate with a system master in a closed loop type system environment. Since the module is internal to the controller unit, it has possible access to all RAM data for transmitting and receiving (depending on the software). The system I/O port (communications inputs) provides additional system detectors inputs and monitor status bits. The RS-232 port (TS-1 version) can be used to interface with LNME series monitors while still maintaining direct dial-up capability through the standard RS-232 port.

There are 3 connectors on the Communications Module:

One 15P NEMA *

One 9P Modem I/O *

One RS-485 (SDLC)

* These are replaced by fiber-optic connectors on the fiber-optic communications module.

The communications module in conjunction with a system master and a personal computer provides the ability to receive system traffic commands and to use the computer, through the system master, to program the controller (download) or to read data from the controller (upload). The computer software provides the ability to compare computer data files with data uploaded from the controller. Differences are highlighted for easy identification of data that has been changed. Printing of data files from the computer can easily accomplished using a standard printer and interface.

LNME INTERFACE

The LMD can interface via its RS-232 port with the LNME series conflict monitor (TS-1 comm module). This feature can be used in either the direct dial or closed loop system context for remote uploads of LNME conflict monitor message logs, compatibility card information, and switch settings.

SPECIFICATIONS

POWER REQUIREMENTS

Voltage	95 to 135 VAC
Frequency	60 + /- 3 Hertz
Power	25 Watts without Ext. + 24 VDC Load 45 Watts with Ext. + 24 VDC Load
Fusing	115 VAC 1 ampere slo-blo + 24 VDC 1 ampere slo-blo
Interrupt	500 milliseconds or less, resume operation as though power interruption had not occurred. 1000 milliseconds or more, revert to initialization routine. 500 to 1000 milliseconds, either resume operation or revert to initialization.
Transient Immunity (high repition noise)	300 volts amplitude @ 2500 watts peak power (1 microsecond pulse rise time, 10 microseconds pulse width) at a repetition rate of 1 pulse every other cycle moving uniformly over the full wave once every 3 seconds for 10 minutes.
Transient Immunity (Low rep,- high energy)	600 volts amplitude from a 10 MFD capacitor once every 10 seconds for a maximum of 10 applications of each polarity.

INPUT/OUTPUT REQUIREMENTS

All logic signals shall be ground TRUE for all DC level input and output terminations when active. Input/Output terminations shall be internally biased to + 24 volts DC when in the FALSE state and not active.

During operation, the controller unit shall not be affected by pulses to the input terminal of 10 microseconds duration 300 volt positive or negative amplitude, and with a maximum repetition rate of 1 pulse per second. The output impedance of the pulse source shall be not less than 1,000 ohms, nor greater than 10,000 ohms.

AC INTERCONNECT CABLE REQUIREMENTS

Cycle 1,2,3,4	2 Conductors
Offset 1	1 Conductor
Offset 2	1 Conductor
Offset 3	1 Conductor
Split 1,2,3,4	2 Conductors
Flash	1 Conductor
System	1 Conductor
Interconnect common	1 conductor
Total	10 Conductors

INPUT CHARACTERISTICS

Transition zone of input circuitry from "low" state to "high" state and vice-versa shall occur between 8 and 16 volts.

A voltage between 0 and 8 volts is considered the "low".e.

A voltage greater than 16 volts is considered the "high".

External transition from "low" state to "high" state and vice-versa shall be accomplished within 0.1 millisecond.

Over the voltage range 0 to 24 volts DC (2 volts), maximum current "in" or "out" of any input control terminal shall be less than 10 milliamperes. Input impedance shall not exceed 10K ohms to 24 volts DC, nor shall the surge impedance be less than 100 ohms resistance.

Any input signal dwelling in a defined logic state for less than 0.25 milliseconds shall not be recognized. Any input signal dwelling in a defined logic state for more than 35 milliseconds shall be recognized, provided successive similar logic state transitions do not occur less than 135 milliseconds apart.

OUTPUT CHARACTERISTICS

"Low state" current sinking shall be at least 250 milliamperes from inductive load.

Any external steady voltage applied to the output terminal shall not exceed 30 colts DC, nor shall it cause flow of more than 3 ma into the terminal, when the output is in the high state.

"Low" operating voltage = 0 to 4 volts.

Maximum transition time = 0.2 millisecond.

"High" state impedance shall not exceed 11K ohms to 24 volts DC.

Any valid output signal shall dwell in a defined logic state for at least 50 milliseconds.

ENVIRONMENTAL REQUIREMENTS

Temperature (Ambient) Operating Range -30°F (-34°C) to + 165°F (+ 74°C)

Humidity (Relative) Not to exceed 95% over the temperature range + 40°F (4.4°C) to + 110°F (43.3°C)

PHYSICAL REQUIREMENTS

Controller Size (allow for front protrusion of connectors)

English	10.5"H x 12.75"W x 9.0"D
Metric	26.7 cm H x 32.4 cm W x 22.9 cm D

BATTERY

The LMD9000 uses a removable 2.4 volt Nicad battery for purposes of power-down clock operation and battery backed RAM. Battery backed RAM is used to retain non-programmed data such as message logs. All *programmed* data is retained in non-volatile EEPROM. The battery will last for a minimum of 10 years during normal controller operation. The battery will operate the clock and retain RAM for a minimum of 30 days without power supplied to the controller.

SECTION II

APPLICATION AND OPERATION

CONTROLLER DEFINITIONS

PHASE

An independent movement of traffic (G,W,Y,R) with its own timing, position within a sequence, and set of compatibilities with other phases.

CONTROLLER UNIT

A controller unit provides timing and logic for phase and overlap control. The controller provides a means of data entry as well as indications of its operating status. The controller responds to inputs and drives outputs based on status of the inputs, user programmed values, and the rules of operation specified by NEMA.

ACTUATED PHASE

A phase that is dependent on vehicle input for service. An actuated phase may be skipped in absence of vehicular or pedestrian demand. If served due to demand, the phase will serve a guaranteed initial period of green (minimum green) followed by extension green periods which are activated by further detector activity.

A call for service indicates that a call for a phase is stored in memory of the controller. If there is a call for the phase, but the phase is not in service (green, yellow or red clearance) then the phase check output of the phase is activated.

A serviceable conflicting call is when one phase is active and there is a call registered for another conflicting phase, such that the other phase is eligible for service--i.e. no omits or other restrictions are applied to it. "Conflicting" indicates that the active phase must clear to service the other phase, i.e. it is not compatible.

PHASE TIME SETTINGS

Minimum green--guaranteed portion of the green

Passage--The time setting that determines the length of extension. Detector inputs reset the passage timer. If it times out before reset, the phase "gaps out".

Yellow--Yellow clearance time

Red--Red clearance time

Max (1 and 2)--The upper limit to green extensions when calls on other phases are present (serviceable conflicting call).

Walk--The walk time setting. If walk is called, the walk indication and this time will go into effect.

PCL--Ped Clearance time setting.

S/A--Seconds per actuation. Used for "variable initial", see volume density.

MVI--Max variable initial, see volume density

TBR--Time before reduction, see volume density

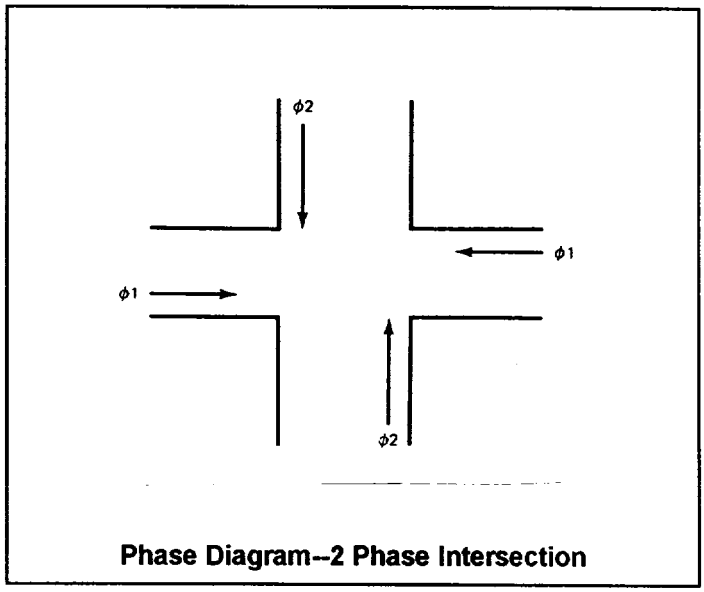
TTR--Time to reduce, see volume density

MINGAP--Min Gap, see volume density

MAX EXT--Time setting for variable MAX time

AUTO MAX--Maximum time setting for variable MAX time.

AMR--Added Max Red time setting for additional red time.



Phase Diagram--2 Phase Intersection

BASIC PHASE SERVICE FEATURES

A phase will be served if it has a call in memory, if the ped or vehicle detector is currently active, or if it is in one of the recall modes. Phases are served in their respective order. When a phase is about to terminate (clear to yellow), the controller will make a "this phase next" decision (TØN) and will commit to the next serviceable phase. If their are no serviceable phases to which the phase can go, it will remain in green in a "rest in green" state until such time as a call arrives, where it will immediately advance to yellow.

Methods of phase service:

1. Actuated by detector input. Two modes:

Memory on. Call is remembered until phase served, even if detector just pulses.

Memory off. Detector input must be active at time of previous phase TØN decision. Used for right turns, etc.

2. Ped input. Phase will service WLK + PCL timing.

3. Recall Extendible (EXT Recall). Phase will always serve phase minimum green. Further green is subject to detector extensions.

4. Recall Max. Phase will always serve phase max time. Detector inputs have no effect.

5. Soft Recall. Similar to recall extendible except phase is only served if no other "real calls" exist. Real calls are those for which there is a detector input actuation.

6. Ped Recall. Ped is always serviced.

7. CNA mode. See CNA definition.

8. Min recall input active. All actuated phases serve min green.

TØN DECISION

The "this phase next decision" is the decision made at the end of the green interval, determining what phase should be serviced next. This decision is based on the sequence in effect and serviceability of the candidate phases in terms of call status, phase omits, etc. Once the controller makes a TØN decision to service a phase, it is committed to do so--phase omits will not prevent that "next phase" from being serviced . Only internal pre-emption, which goes through a special process (largely because of overlaps), can override a this phase next decision.

DETECTOR DELAY

Pertains to call phase, during red only. The detector zone must be continuously occupied during the delay period for a call to be placed on the phase (whether memory is on or off). The delay timer times down during the red of the call phase only when the input is active (LOW). If the input goes HI, the delay timer is set back to its full value. A call will be placed after the timer times out. Memory on/off status would have an effect at this point. Detectors must operate in the **presence** mode with delay.

DETECTOR STRETCH

Pertains to the EXT/SW phase(s) during the green only. Stretches the end of the pulse by the programmed value. The stretch timer times down during green when the input is HI after it has gone Low. The controller acts as if the total pulse lasts for the pulse + stretch duration (PSG is held at full value until stretch times out).

DETECTOR DISCONNECT

Pertains to CALL phases only, during green. The disconnect timer is held at full value during green, and and the input is active (low). If not active (high) the timer times down and the detector input will be effectively disconnected or unresponsive to further activity. This would typically be used in place of a "calling only" detector at the stop bar (in conjunction with an extending set-back detector). In the case of a calling only stop bar detector, the waiting vehicle queue (ahead of the extending set-back detector) could not extend green time beyond the Min time.

DELAY ENABLE

The delay timer only times if the enable phase is green. Typically used with 5 section head protected/permissive left turns on the main street to enable the delay only when in the opposite thru green (e.g.. ph 2 is the enable for ph 1's delay). This prevents a resting main from immediately terminating when a left turn actuation arrives...yet prevents skipping a late arriving left turn when cycling around from the side street.

Note: Special logic is provided in dual ring operation so that, after the delay, **both** thru's will terminate even if returning back to just one left turn. The adjacent thru will then red-revert back to green. This is done to prevent vehicles from being trapped and for safety (since opposite turn drivers tend to assume that both sides will clear).

DETECTOR FAIL MONITOR

Detector Failure Monitoring can be used to determine if selected detectors have malfunctioned over a settable sampling period. Detector failures can programmed to simply generate a log and take no action (see Reports), or, they can be programmed to place a selected phase in **"Max Fail Recall"** (MFR) as well. In this mode, the phase will be placed on recall using the Fail Max time value in the Max Plan (Max plans must be used for MFR). Thus, if the detector fails, the phase is placed on recall using a second special max time (usually shorter than the normal max).

There are 4 failure modes:

No activity--no calls over the sampling period
Under threshold--under a specified number of counts
Over threshold--over a specified number of counts
Constant call--detector input low over entire period

If a failed detector returns to within normal operation on a subsequent sampling period, it will be removed from failure status while the phase will be returned to normal operation (removed from Max Fail Recall if in that mode).

The **no activity** and **constant call** monitors can be inhibited by clock circuits. However, these ckt's cannot clear a detector failure if already failed prior to circuit activation.

DETECTOR SIMULATION

Detector Simulation allows the controller to simulate detector calls. With this feature, the controller is capable of simulating an operating intersection. Calls are generated based on a user defined SATURATION RATE (Vehicles per Hours,VPH) and a PERCENT OF SATURATION, the result of which is a TOTAL VOLUME. As an option, it is also possible to simulate speed (with a user definable pulse width) and waiting vehicle queue.

This feature can operate on a "system level" only, where system detector data is provided, but there is no calling or extending of phases (for use at live intersections). It can also operate on an "input" level where phases are called and extended as well as providing system level data.

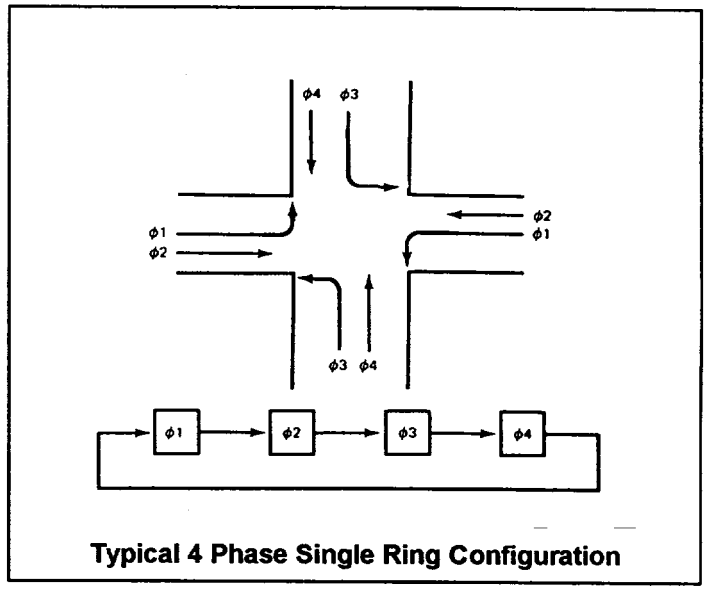
CNA MODE (Call to Non-Actuated Mode)

The CNA mode provides a special mode of non-actuated (always served) phase operation. Call to non-act mode is implemented by one of two inputs, CNA I, CNA II. The phases served are determined by user assigned phases for each input. One, two or any combination of all 8 phases may be assigned to each input. When the input becomes active, the phases assigned go into the special Call to Non-Act mode. When not active, the phases are served in their normal fashion.

When in the CNA mode, the phase will always serve the Walk plus Ped Clear time, and detector inputs will have no effect. The difference between CNA mode and a normal Ped call has to do with the hold input. When hold is applied, the CNA phase will hold at the end of walk until released. whereas hold applied to a normal ped called phase will hold at the end of ped clearance. The obvious difference is that, when hold is released, the CNA phase would have to time the ped clearance interval before advancing to yellow whereas the ped called phase would immediately advance to yellow.

RING

An ordered sequencing of mutually exclusive phases. Only one phase may display right-of-way indications (G,W,Y) at any one time. Phases sequence in order from phase 1 to 2 to 3, etc., back to phase 1 after the last phase is serviced. Phases can be skipped if no demand exists.



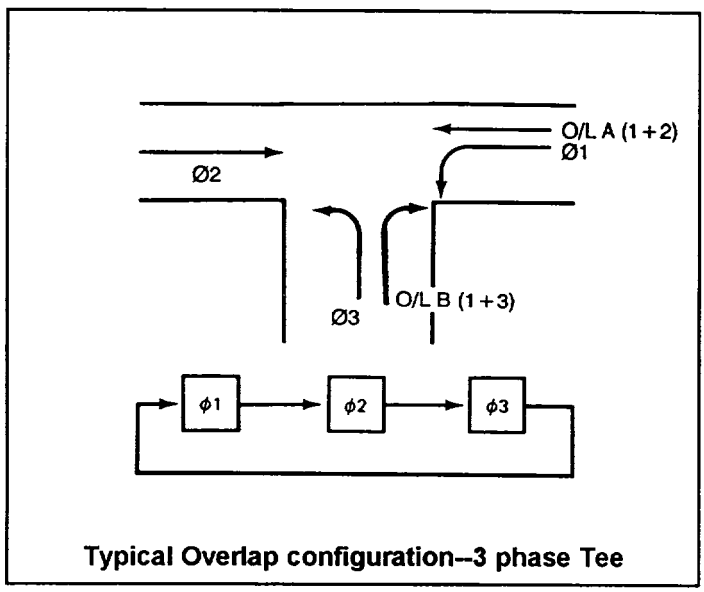
Typical 4 Phase Single Ring Configuration

SINGLE RING

One ring, one phase at a time in a prescribed order.

OVERLAPS and OVERLAP FEATURES

An overlap is an independent movement of traffic but depends on other phases, referred to as "parent phases", for its operation and timing. The overlaps are generated by 4 sets of generic overlap drivers labeled O/L A, B, C, and D. Each set consists of a Red, Yellow, and Green output, the user programs the overlap parent phases. For example, say that O/L A is set up as a 1+ 2 overlap, i.e. it overlaps phases 1 and 2. When either phase 1 or 2 is



Typical Overlap configuration--3 phase Tee

green, overlap A is thus green as well. In addition, if phase 1 clears directly from phase 1 to 2 or directly from 2 to 1, the overlap will remain green through the clearance period, and through the next phase green. If, however, the next phase is not part of the overlap, say phase 3 in this case, the overlap will clear (i.e. time yellow and red) with the clearing parent phase. The overlap outputs "borrow" the yellow and red clearance timing from the clearing parent phase. It is important to realize that the controller must decide what to do with the overlap before it begins clearances. Overlaps are largely responsible for the "this phase next decision" --the controller must decide and commit to a phase at the end of the previous green.

'Not Ped" overlaps

Not ped overlaps would typically be used where right turn overlaps conflict with peds. A "Not Ped" overlap parent phase is considered an overlap if there is no ped call, *it is not* if there is. If ped service is required, the overlap will clear and remain red until ped service is complete (WLK+ PCL). If the phase remains green after ped service (extensions, etc.), the overlap will return to green (5 second minimum guaranteed). If the "Not Ped" phase rests green/DW, the overlap will display green. A ped call on the phase will then clear the overlap, time the ped, then return to overlap green (if not an actuated-rest-in-walk type ped). If the "Not Ped" overlap phase clears to a non-overlapping phase right after ped service, the overlap will remain red.

PHASES AS OVERLAPS

Programming of this section allows the normal NEMA phase outputs to be programmed as overlaps. When programmed with all zeroes, the LMD reverts to standard NEMA operation. This is the default state when shipped from the factory or as a result of clear or back-up copy codes. Otherwise, a "1" programmed under a specific phase indicates that the phase is an overlap parent phase.

DUAL RING

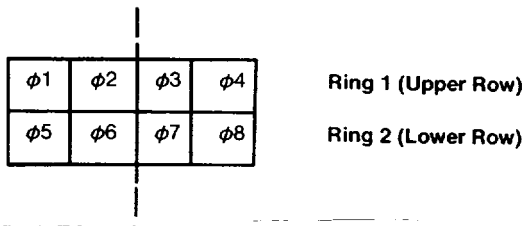
Two rings, 2 phases can display right-of-way indications at the same time (concurrently). Phases timing together are confined to a prescribed set of compatibilities and sequencing.

COMPATIBILITY LINE (OR BARRIER)

The dividing line crossing both rings that separate compatible phase combinations. Usually it divides phases associated with one street, say East/West, vs. another, say North/South.

BARRIER PHASE

Any phase for which the next phase in service is on the opposite side of the barrier. In the standard NEMA dual ring sequence, 2,6,4,8 are barrier phases. Note that if the normal barrier phase is not serviceable (no call, omit, etc.) the preceding phase assumes the same characteristics of a barrier phase.



Compatibility Line (or Barrier)

RULES FOR STANDARD DUAL RING OPERATION

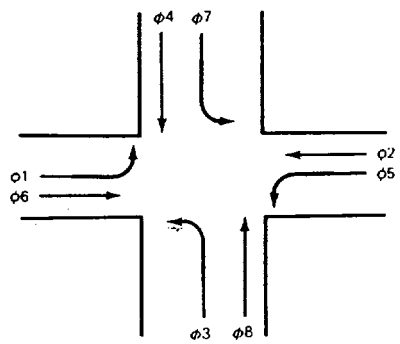
1. No two phases in the same ring can time together

2. Phases in one ring can time with any phase in the opposite ring so long as it is on the same side of the barrier. In the standard NEMA dual ring sequence, the allowable combinations are:

1-5, 1-6, 2-5, 2-6, 3-7, 3-8, 4-7, 4-8

3. All phases on one side of the barrier must clear through red clearance before crossing to the opposite side of the barrier.

4. If the barrier phase green in one ring continues to time while the barrier phase in the opposite ring has timed out, the timed out phase green will go to a "rest" state, subsequently clearing when the other phase times out. The phase preceding this phase will behave the same way if there is no call on the normal barrier phase or it is not used.



TYPICAL NEMA 8 PHASE QUAD LEFT TURN
(Example of dual ring phasing)

5. One phase at time may be served in a dual ring configuration. If so, any compatible phase in the opposite ring is eligible for immediate service. However, if "Dual Entry" is in effect, two phases at time will be served where, in the absence of a "real" call in the opposite ring, the controller will place a call (user defined).

SEQUENCE SELECTION

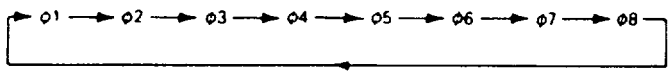
The LMD is capable of a variety of sequences for sequential and dual ring timing. The selection of the desired sequence is accomplished by programming through the keyboard. See section III for programming details.

The following sequence patterns are available as determined by the indicated programming codes.

AVAILABLE SEQUENCES

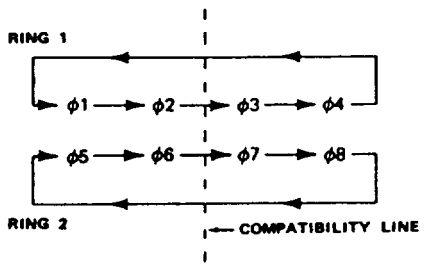
The LMD controller is capable of a variety of basic sequences, including single ring, dual ring, and combinations of single and dual ring as follows.

Sequential. Only one phase allowed service at a time. Menu selection 1.



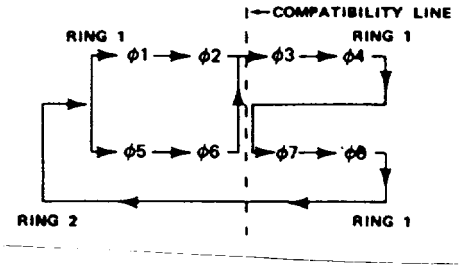
NEMA Dual Ring (4 over 4). Menu selection 2

Two phases allowed service at a time, as follows:

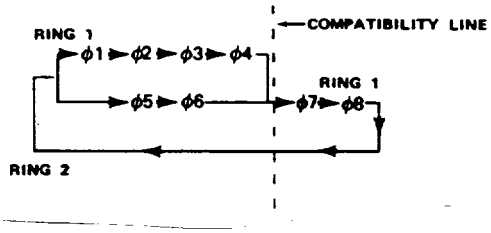


The compatibility line is a boundary which prohibits concurrent right of way timing of phases from the left side of the line with phases on the right side of the line.

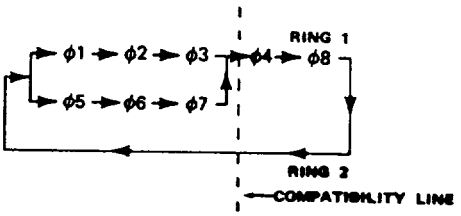
Special sequence # 1, dual left side, sequential right (2 over 2 plus 4). Menu selection 3.



Special sequence # 2, 4 over 2, plus 2. Menu select. 4

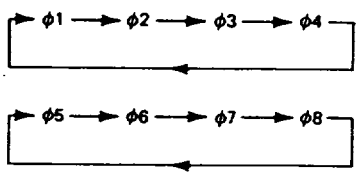


Special sequence # 3, 3 over 3, plus 2. Menu select. 5

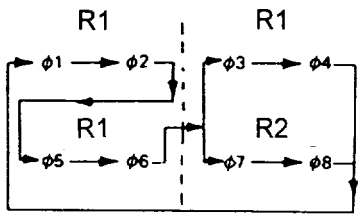


Special sequence # 4, 4 over 4, no barrier. Menu sel. 6

This sequence would operate as two independent 4 phase controllers.



Special sequence # 5, left side sequential, right side dual ring (4 plus 2 over 2). Menu selection 7



Note 1:
A new phase sequence pattern will be recognized only at "initialization". Initialization occurs on power-up, external start, or keyboard re-start. If the controller is not re-initialized, the old sequence will prevail until the unit is re-initialized.

Note 2:
The initialization phases and the flash entry/exit phases should be consistent with the sequence selected.

ALTERNATE SEQUENCES (LEAD/LAG OPERATION)

Alternate Sequences make it possible to reverse the phase sequence on a phase pair basis. The phase pairs are 1-2, 3-4, 5-6, 7-8. When reversed, the odd phase will lag the even phase instead of leading it as is normal. Any combination of the phase pairs may be reversed. Since there are 4 pairs and each can be reversed or not, there is a total of 16 sequences available. The sequence selection may be made by input (ALT SEQ A-D) selection, associated with a certain combination of cycle/split, or Timing Plan.

CONDITIONAL SERVICE/RE-SERVICE

Conditional Service is a mode of dual ring operation in which an odd phase may be allowed re-service after the even phase but prior to crossing the barrier. When conditional service is in effect, re-service for an odd phase is allowed under the following conditions:

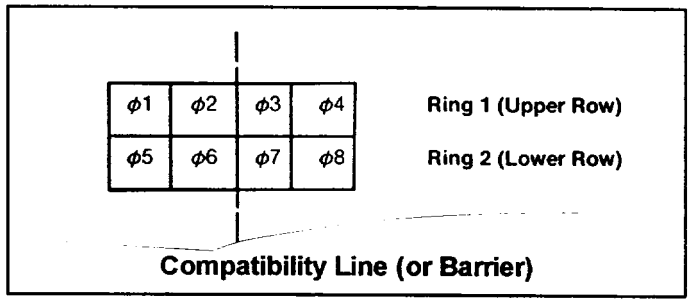
1) The even phase in the same ring has gapped out and is resting.

2) There is a call across the barrier (otherwise conditional service is unnecessary).

3) The even phase in the opposite ring is still extending and there is enough time left in its max timer. This time must be equal to or greater than the special "conditional service max timer" plus the even-phase-same-ring's clearance time.

When a phase is conditionally serviced, it cannot extend beyond the special conditional service max time. When it clears, it will cross the barrier with the opposite ring even phase. The same ring even phase will not be serviced again in that cycle.

For example, consider the standard NEMA QLT phase sequence diagram:



Now, suppose Conditional Service is in effect for phases 1 and 5. The conditional service max time is set at 10 seconds, while phase 2 and 6 have 30 second max times. Phases 2 and 6 each have a total of 5 seconds clearance:

a. Assume 2 and 6 are currently in green and extending, and there is a call for service across the barrier.*

b. Say that phase 6 gaps out at the point where phase 2 has timed just 15 seconds of its max time.

In this case, there is just enough time to conditionally service phase 5 because there is still 15 seconds left in the phase 2 max timer. This is just equal to phase 6 clearance (5) plus the conditional service max time (10) and therefore just enough to allow conditional service. Had there been any less than 15 seconds left in the phase 2 max timer, conditional service would not have been allowed. Note that although the conditionally serviced phase now has a 10 second max timer, it could always gap-out before that point.

* The reason that a call across the barrier is stipulated is that if there is no call, the controller would return to phases 1 and 5 anyway, even without conditional service.

Conditional Reservice

Conditional Reservice allows return to the thru phase after the conditionally serviced left turn, otherwise stay in left turn then clear to serve cross street phases. Max times apply.

SIMULTANEOUS GAP-OUT INHIBIT

As discussed previously, all phases on one side of the barrier must wait for one-another before crossing the barrier (they clear together). For instance, if phase 2 gap's out but 6 is still extending, then 2 will rest in green. Not only will it rest, but in the normal NEMA mode, its passage timer can reset and begin timing again. In other words, a phase could rest until the opposite phase was just about to gap out, receive a detector actuation, then be extended. This could happen back and forth between the rings and could effectively lengthen the gap, making

the phase termination sluggish. Ultimately, both phases would have to "simultaneously gap out" in order for either to gap out and actually begin clearance..

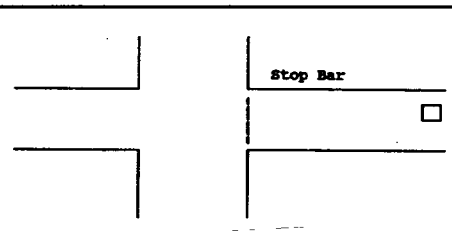
Simultaneous Gap-out Inhibit simply disallows a phase's passage timer from starting up again once it has timed out completely. This generally results in "snappier" operation since, once a phase gaps out it stays that way, and, as soon as the other ring gaps out, the barrier is crossed.

VOLUME DENSITY

The term "Volume density" in NEMA controllers actually incorporates two separate processes; Variable Initial and Gap Reduction.

Variable Initial. Allows the minimum green period to be extended depending on the size of the waiting vehicle queue. It is Controlled by the Seconds per Actuation (S/A) setting. It Operates when the corresponding phase is Red. When a vehicle passes over the detector, the variable initial tabulation begins, each successive actuation adding to the previous. The tabulation begins at zero and will only lengthen the minimum green period when the sum exceeds the normal min green setting. For example, say the normal minimum green is 5 seconds and the seconds per actuation setting is 2 seconds. Only after the third actuation (during red) when the sum is 6 will the minimum green be lengthened. Each additional S/A actuation will then lengthen the min green by 2 seconds (8, 10, 12, etc.), possibly up to the MAX Variable Initial setting.

Note that S/A can only be meaningfully used if the detector is back from the stop bar. Otherwise, no vehicles would pass over the detector during Red.



Set-back or Advance Detector

Gap Reduction. Allows the gap (passage timer value) to be reduced during the green of the phase.

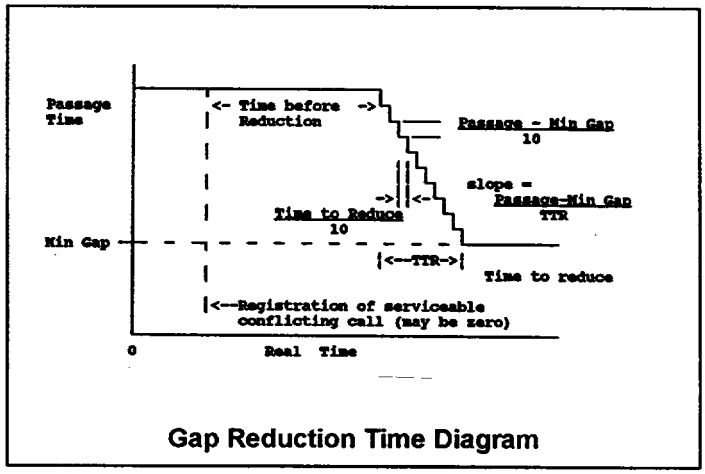
The reduction period does not begin until the Time Before Reduction (TBR) timer times out. Once it begins, it will always reduce in 10 equal steps. The time taken for the total reduction process is equal to the Time to Reduce (TTR) setting. The Min Gap is the lowest level to which the passage timer (gap) will reduce.

When the phase gaps-out at reduced gap, one of three things occurs, depending on programming:

-If last car passage is in effect, the controller commits to gapping out, but will time one full passage timer for that last car.

-If last car passage is not in effect, but "guaranteed re-service" is in effect, the phase is placed on min recall for the next service.

-If the third option is in effect the unit will not last car passage or place a call to return to the phase



Gap Reduction Time Diagram

Gap reduction Note

Gap reduction with last car passage has been traditionally used at high speed intersections in an attempt to prevent vehicles from being caught in the "dilemma zone". How-ever, gap reduction can also be an effective way to begin the phase with a fairly long passage time when vehicles are moving slow, then move to a shorter time later when they are moving at the flow rate. Gap reduction is thus a good way to obtain snappy operation without complaints--which is often the case if passage values are simply set low, especially as they apply to the beginning of the phase.

To use gap reduction for this purpose, you may find these settings useful:

Passage = 4 to 8 seconds (i.e. rather long)
TBR = Min Green + 5 to 15 seconds
TTR = Anywhere from 10 seconds to Max Time-TBR*
Min Gap = .5 to 2.5 seconds (i.e. rather short)
Last car passage = off, guaranteed re-service = off

*For example, if TBR = 15 and Max = 45, you might set TTR at 40 - 15 = 25.

AUTO MAX/MAX EXTEND OPERATION

The Max Extend and Auto Max feature provides per phase variable max operation based on vehicle demand. The feature is enabled when non-zero values are programmed for both Max extend and Auto Max (Auto Max must be higher than any used max's). When programmed, one Max Extension will be added to the current max whenever the phase max's out twice in a row. Conversely, one Max Extension will be subtracted from the current max whenever the phase gap's out twice in a row. The Auto Max value provides the upper limit and the current *programmed* max value provides the lower limit (including Max Plans if used).

ADDED MAX RED

The Added Max Red feature provides per phase additional red time to normal phase red time after a max-out or force-off. This feature would normally be used with "dilemma zone" avoidance systems. Such systems employ loops set back behind the dilemma zone which extend vehicles through the dilemma zone as well as the intersection itself. These systems, however, normally break down when the phase Max's out or forces off. The last vehicle may have to make a dilemma zone decision. ADDED MAX RED adds a programmable red value to the normal red under these circumstances for an extra margin of clearance. This feature is not active on gap-outs and the red time is reset to normal after each clearance.

PEDESTRIAN FEATURES

ACTUATED REST IN WALK

Selectable per phase. When ped serviced, it rests at the end of walk until a serviceable conflicting call is registered. Walk rest modifier is not necessary for actuated rest in walk.

CONDITIONAL PED SERVICE

Conditional Ped Service allows up to two ped services after the start of green. If there is no call for ped service at the beginning of green, green/don't walk would be displayed. If time permits (Max timer), up to two late peds can be served per cycle. If the first ped movement is in ped clearance, a new ped call would cause an immediate return to walk.

DUAL ENHANCED PED

Enabled by a clock circuit and applies to dual ring controllers with peds on opposite ring thru (even) phases. When activated, if both thru's have ped calls, but if one ped starts before the other, that ped will "rest" at the end of walk until the other walk comes up and times out. The "rest at the end of walk" state will *not occur* unless there is an opposite ring ped call. For example, say the LMD goes to 2 and 5, with ped service on 2. Say there is a ped call on 6. Phase 2 will then rest at the end of walk until phase 6's walk times out. Both phases will then time ped clearance together.

ENHANCED PED

For CNA I phases. When Enhanced Ped is enabled but CNA I is not active, CNA I phases will time walk with the Max I value. When CNA I is active, the phase will time according to the normal NEMA requirements of CNA phases using the normal walk setting.

EXCLUSIVE PED

Exclusive ped operation can be provided full time or on a time of day basis. When in operation, peds on phases 2, 4, 6, and 8 time simultaneously and exclusively (no greens on during Walk or PCL).

FLASHING DON'T WALK THRU YELLOW

When enabled, will flash the Don't walk indication thru yellow. It will go solid at the end of yellow (instead of at the end of green).

FLASHING WALK

When enabled, will flash the walk indication. The WALK indication would flash at 1Hz if active, otherwise PED indications are normal.

FLASHING WALK THROUGH PED CLEARANCE

This feature flashes the WALK indication at the same time as PED CLEAR. The WALK indication would flash at 1Hz if active, otherwise PED indications are normal.

PEDESTRIAN OMIT

The PED OMIT input inhibits the selection of a phase due to the presence of a pedestrian call on that phase and prohibits the servicing of a pedestrian call on the phase even though the phase may be serviced in response to a vehicle call. Activation of the input does not affect a pedestrian service in the process of timing at the time of its application.

PED OVERLAPS

PG DWN from previous screen. Allows ped drivers to be set up as ped overlaps, i.e. to begin in one phase and end in another. Recall that phase overlaps are based on a *"this phase next"* decision at the end of green to determine how to process vehicle overlaps. Similarly, ped overlaps make a *"this ped next"* decision to determine how to process O/L peds. If the next phase *is an overlapping ped phase* and *has a* ***ped call***, the walk will be maintained into the next phase. Ped clearance timing *may* be skipped if not needed (see note). If the next phase is *not a ped overlap* phase, or *does not have a ped call* registered at the end of the current phase walk, the phase will time ped clear normally. If the call is registered *after* ped

clear has begun, the ped will terminate normally, then begin walk again at the beginning of the ped overlap phase green. All overlap ped timing is subject to the active phase.

NOT PED OVERLAPS

O/L parent phases can be programmed as "not ped" overlaps. In this mode, the phase is considered an overlap if there is no ped service, but not if there is. Typically used with right turn arrows to prevent displaying the arrow into peds. The LMD "not ped" overlap has advantages over most other "negative ped" overlaps in that the overlap (arrow) can return for the duration of the phase after ped clearance is timed. A built in minimum of 5 seconds is assured. However, if the phase ends right after ped service and skips to a non-overlapping phase, the overlap (arrow) never comes on. Also, if the phase rests, the arrow will remain on but will be cleared if the ped is re-serviced. Programmable yellow and reds are provided for this.

PEDESTRIAN RECYCLE

This input is designed to control the recycling of the pedestrian movement. The response of the controller unit is dependent on whether the phase is operating in the actuated or non-actuated mode.

1. **ACTUATED MODE.** If a serviceable pedestrian call exists on the phase and the HOLD input is active, the pedestrian movement will be recycled when the Pedestrian Recycle input is active regardless of whether a serviceable conflicting call exists.

2. **NON-ACTUATED MODE.** If the phase has reached the Green/Dwell/Select state (STATE D), the PED OMIT input is not active on the phase, and a serviceable conflicting call does not exist, the pedestrian movement will be recycled when the Pedestrian Recycle input is on.

NOTE: The term "pedestrian recycle" is understood to be any start of pedestrian service after the start of phase green; i.e. a late ped service start or a 2nd ped service.

WALK REST MODIFIER

This input is capable of modifying the operation of a non-actuated phase only. When active, all non-actuated phases will remain in the timed out Walk state (Rest-in-Walk) in the absence of a serviceable conflicting call without requiring the Hold input to be active. Also when active, the controller unit will recycle the pedestrian movement upon reaching the Green Dwell/Select state (State D) in absence of a serviceable conflicting call. When not active, non-actuated phases will not remain in the timed out Walk state unless the Hold input is active.

OTHER IMPORTANT FEATURES

5 SECTION HEAD PHASE RESTRICTIONS

There is a provision in the LMD to prohibit certain sequencing of the controller when protected/permissive 5 section head control is used. Specifically, the LMD can be programmed to restrict return to leading left turns directly from the thru movement. For example, 1& 5 could be restricted from service directly from 2 & 6, without first serving intermediate phase(s) on the side street. The idea is to disallow return to the protected arrow if there is no call for side street--since the left turn traffic has a permissive option.

ADVANCE WARNING LOGIC

Advance warning consists of a per movement output that activates when the normal movement decides to terminate by gap-out, max-out, force-off, etc. The *actual termination* of the movement green is then delayed for a user definable period during which the advance warning output is active. The output remains active through yellow and red until the phase/overlap once again returns green and the Advance Warning De-activation Delay times out (ADD). The advance warning outputs are the time clock ckt outputs 1-12, enabled when a phase as overlap or overlap has the AW feature ON. *Internal selection* of time base coordination functions are unaffected by this operation, as only the *physical* outputs are used.

INCREASE YELLOW & RED

Increase Yellow & Red is a special function that allows all yellow and red intervals to be increased by up to 100 per cent. The increase is enabled by Clock CKT 148. For example, if Yellow and Red are normally 4 and 2 respectively, and IY & R is 50%, then upon activation of CKT 148, Yellow will time 6, and Red will time 3.

Note: We do not recommend using I Y & R for routine circumstances like night versus day, as drivers may become accustomed to one set of timings versus another. Instead, the intent is for I Y & R to be activated under special circumstances like inclement weather conditions. This can be accomplished by activating CKT 148 only during a special day program (or programs) which is/are assigned to week 10, remotely activated by input (see week programs).

TIME CLOCK

The LMD is equipped with internal time clock as a standard feature in all units. The LMD internal time clock is yearly programmable, consisting of programmed events which are assigned to day programs (24 hours), day programs being assigned to week programs (7 days), and week programs being assigned to a year program. The real time clock operates on a 99 year calendar.

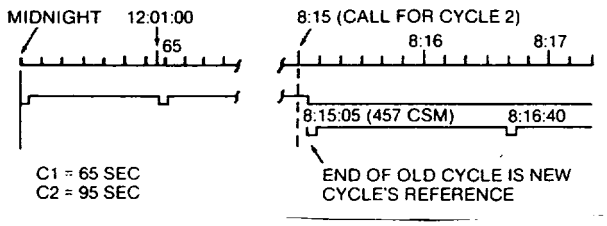
Time clock coordination control - When enabled to do so, the time clock is able to control the coordination command set, thereby selecting the cycle, split, offset and system/free status in effect based on day program event selections.

Timing Plans - various combinations of cycle, split, and offset can be assigned to a set of timing plans. Time clock event programming will then assign these plans to be implemented on a time of day, day of week basis simply by plan number, without necessity of individually programming circuits.

Sync reference modes - The coordination cycle in effect, when selected by time clock, is referenced to the time clock by means of a time base reference (not an input). The LMD will automatically correct the cycle counter upon power-up as well as on command to the time base reference. To provide flexibility in adapting the unit to synchronize to other types of units, the LMD provides four keyboard selectable methods of sync referencing as follows:

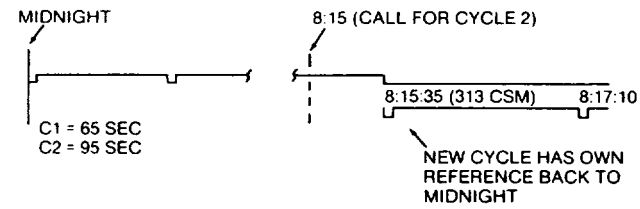
End of previous cycle -This is a daily reference method such that the cycle in effect at midnight will reset and subsequently reference to midnight. Upon any further cycle event change, the unit will, from the event change point, continue its current cycle until completion. The new cycle will begin and reference to the end of the previous cycle. Because it is at the end of the cycle, this method does not require offset seeking when a cycle only change is made.

The figure below illustrates the transition of cycle 1 (65) to cycle 2 (95) using the end of previous cycle method, where cycle 2 is called for at 8:15 AM.



Eight Independent daily reference - This is a daily reference method such that each of the 8 cycles will have their own programmable time of day reference point. Each cycle will be reset at this time each day and subsequently referenced to this time. When a cycle event change occurs, the unit will seek to the new sync pulse which has its own reference, without regard to the old cycle. This method is event history independent in the sense that any two units calling for the same cycle will be in step regardless of their particular event histories or time of event occurrence.

The figure below illustrates the transition of cycle 1 (65) to cycle 2 (95) using the 8 independent method, where cycle 2 is called for at 8:15 AM.



Absolute reference - This is a non-once-per-day reference method in which each cycle is individually referenced to a single point in time by a keyboard initiated reset command. The unit will continuously update its reference from this point on a cycle by cycle basis. After a power outage, the unit will automatically reference each cycle counter back to its last reference point. The LMD is capable of automatically referencing back a minimum of 100 hours after power outage without manual reset. Without power interruption the cycle timers will free-run without daily without interruption (as would be the case in daily reference techniques). This method allows the LMD to keep step with a free running cycle counter, particularly one which does not evenly divide into 24 hours such as a 70 second dial unit.

Event reference - In this method the LMD references the cycle counter to the beginning of the time clock event calling for that cycle, inclusive of when an event calls for the cycle already in effect.

Daylight savings adjustments - The LMD provides an enable/disable option for daylight savings adjustments. When enabled, the unit will automatically adjust daylight savings: forward on the first Sunday in April and back on the last Sunday in October. When disabled, the unit will make no daylight savings adjustments.

Exception days - Exception day programming assigns a selected day program to a particular day of the year which will override the normal programming for that day. To provide the ability to program exception days that are suitable for any year, two types of exception days are provided:

Day of week, week of month, month of year specific exception days. This type of exception day accommodates holidays such as Memorial day, which is the last Monday in May, or Labor day which is first Monday in September, etc. These shall be programmed by DOW, WOM, MOY, since they do not fall on the same date every year.

Date specific exception days. This type accommodates holidays such as Christmas, Jan 1, the 4th of July, etc. These are programmed by date, and fall on the same date each year.

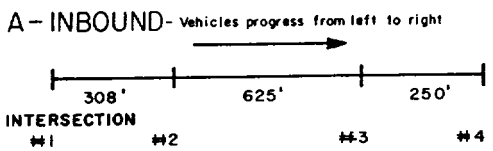
The LMD time clock may be set for the correct time to the correct hour, minute, second, year and date. Each output function is capable of being programmed in increments of one second.

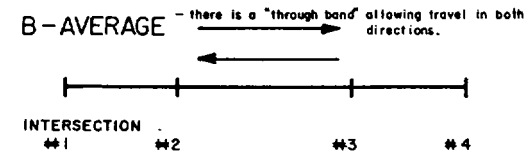
Max II/CNA select by clock - The LMD provides a programming option to automatically select Max II and/or CNA after the unit enters system operation. This feature is internally accomplished without need of external wiring.

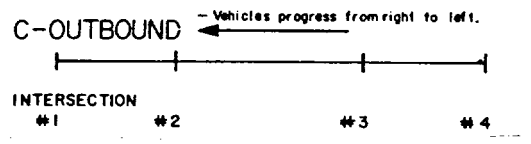
INTRODUCTION TO COORDINATION

Coordination of traffic signals is a term used to describe a process in which two or more intersections are synchronized so that vehicles can pass through each intersection without stopping.

Coordination is accomplished by synchronizing each coordinated phase(s) (Main Street) green of each intersection to a system reference point, or master sync pulse. Each intersection is "offset" from the system reference by a value calculated to account for vehicle travel time. This value is referred to as the offset value and usually differs from intersection to intersection. Intersections set up this way will establish what is called "progression" of signals. There are three basic types of coordinated progressions. For example, consider the following intersections with the indicated progressions.

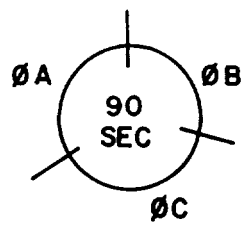




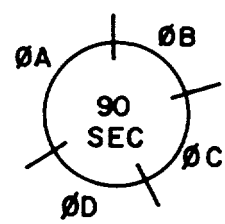


Differences in the offset values of each intersection determine the type of progression. In order for synchronization and therefore the progression to be a continuous process, the return to the artery green of each intersection must be on a cyclical basis. This cycle, or time to serve all phases, must be the same for all intersections within the system.

A Cycle Length is the total time to serve all phases. Both intersections shown have the same cycle length (90 seconds).

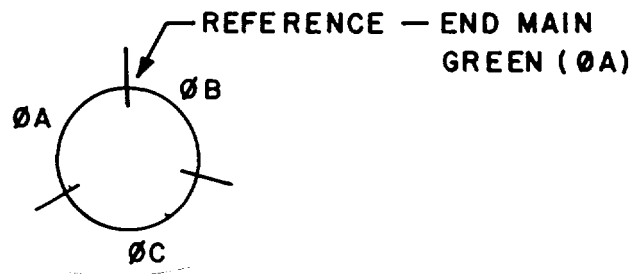


INT. #1-3 PHASE



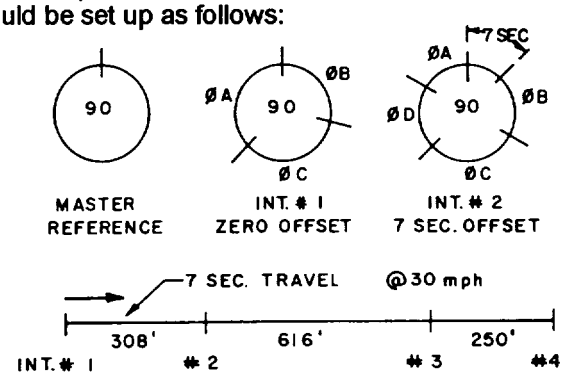
INT. #2 - 4 PHASE

A split is the division of phases within the cycle. Note that the phasing of intersection # 2 and also the split is not the same as intersection # 1. However, since both have the same cycle length, synchronization can be accomplished. Each intersection has a reference point to synchronize to. Usually the start or end of Main Green.



This is the point that is used to reference to the master reference.

The master reference then establishes synchronization. For example, for an inbound off set, intersections 1 and 2 would be set up as follows:



Intersection # 1 has zero offset–it is the master intersection. The master reference issues the reference signal.

Intersection # 2 is offset 7 seconds to allow for travel time. Each successive intersection has an offset value determined by the travel speed and distance.

A traditional reference is a 3-second pulse of zero volts from a 110VAC signal.

All intersections reference themselves to these "Sync Pulses".

However, over the years other methods of providing referencing sync pulses have been incorporated. One of which is "time based coordination" in which each controller internally issues its own reference pulse based on the exact time of day, day of week, week of year. Another method is through the communications link in which a system master transmits the sync pulse as an encoded signal.

Regardless of the form of the sync pulse, the concept is still the same, the local cycle references to the master sync pulse. The process of getting in the proper relationship of the local cycle to the master sync is called offset seeking".

COORDINATION OF AN ACTUATED CONTROLLER UNIT

In this discussion of COORDINATION thus far, no mention has been made of the various types of controllers, specifically pretimed controllers versus actuated controllers. In a pre-timed controller the cycle length is fixed and does not vary from cycle to cycle.

Thus, if any point within the cycle is synchronized, the entire cycle must be synchronized as well. Therefore, to synchronize a pre-timed controller, one need only to worry about the synchronization process and the cycle length selection of each controller.

When we consider an actuated controller, however, just the establishment of a cycle length is a considerable process in itself. This is because the cycle length of an actuated controller will normally vary from cycle to cycle depending on vehicle demand. A cycle length must then be "artificially imposed" on an actuated controller to obtain coordinated operation. To accomplish this, there are certain functions that the LMD coordinator uses, such as permissive periods, holds, and force offs. These functions force the controller to operate within the constraints of a "background cycle" while still allowing the controller to operate in the actuated mode.

LMD COORDINATION

The LMD controller is capable of the following coordination features:

- Eight cycles
- Four splits per cycle or 32 Timing Plans (TS-2)
- Five offsets per cycle
- Eight permissive periods per split
- Eight force-offs per split
- One pedestrian permissive, or automatic permissive
- One dwell period per cycle

Coord Modes Selection

The source of selection of the Timing Plan (or cycle/split), offset, flash and system commands is selectable through the keyboard (under coordination, coord modes menu). Choices are; Manual, Time Clock, AC interconnect, FSK communications with time clock backup (closed loop system), or AC interconnect with time clock backup (the Interconnect inhibit input or clock ckt 54 active disables the interconnect and allows clock operation).

Master vs. Local Cycle

The "background cycle" is often called the "local cycle" because it supervises the timing of the local phases of the controller. In addition to the local cycle, the LMD has a "master cycle" which is a function of the method of coordination. The master cycle could be referenced to an interconnect, FSK communications, or an internal time base reference.

The local cycle, in turn, references to the master cycle by an offset value. Whichever method of coordination is chosen, the master cycle should be step with all units in the system. Also, the master and the local cycle would always be the same value at any one time. The local cycle, however, may be offset from the master cycle by individual amounts at each intersection.

Coordinated phases

One or two phases (single vs. dual ring) are designated as the coordinated phase(s). A set of coordinated phases are assigned to each cycle/split combination, to be implemented upon activation of that cycle and split.

The coordinated phase in effect during coordinated operation is treated specially:

(1) hold will be applied to the coordinated phase(s) when no permissive period is active, and

(2) the coordinated phase does not require a permissive period, in fact, the permissive operation for all other phases is conditioned by the coordinated phase(s)--see permissive explanation.

Permissive periods

Permissive periods restrict service to non-coordinated phases to certain portions of the background cycle length in order to assure that they are not serviced late and therefore can meet their force off obligations. The beginning of the first permissive period is often called the "yield point", as it determines when the coordinated phase(s) will "yield" to other phases. During each permissive period, the coordinated phase(s) selectively responds to vehicle and/or pedestrian calls by the de-activation of phase omits.

Each permissive period has a starting and ending point within the cycle, programmable on a per split basis. Permissives periods are associated with specific phases. When the permissive is active, the associated phases are permitted.

When the permissive is not active, and the coordinated phase is green, phases associated with the permissive output would be omitted and not eligible for service. It should be noted that permissives only have an effect when the controller is in the coordinated phase. Permissives are immediately inhibited for the associated ring as soon as any non-coordinated phase green begins--all phases in the ring are allowed.

Any time there are no permissive periods active, hold is applied to the coordinated phase(s). Thus, if the LMD is in the coordinated phase, but prior to activation of any of the permissives, hold is applied to the coord phase(s) and omit is applied to all non-coordinated phases. When the start of the first permissive occurs, phase omits are released on the corresponding phases which allows them service. When the end of permissive occurs, if the controller is still in the coordinated phase green (say there was no demand), phase omits will be re-applied. If any non-coordinated phase is serviced, all other phases in that ring are also eligible for service.

PERMISSIVE NOTES.

1. The reason that permissives have no effect after leaving the coordinated phase green is as follows. Suppose that in an 8 phase NEMA configuration, the coordinated phases are 2 and 6 and the first permissive period is permissive to phases 3 and 7 only (many choose to do this). The permissive for 4 and 8 would then start sometime later. The idea here is; if there are no calls on 3 and 7 at all, the controller will stay in the coordinated phase until 4 and 8's permissive.

The problem would occur if the controller leaves to serve 3 and/or 7 and those phases subsequently gap out early--that is, before 4 and 8's permissive starts. If the permissives were not rendered ineffective at this point (before 4 and 8's permissive comes up)--the controller would have no choice but to return to the coordinated phase. Phases 4 and 8 would probably be skipped altogether...a most undesirable situation.

To avoid this, once a non-coordinated phase green is started, all omits are dropped and all phases with calls are served in order. This is acceptable because, if permissives are set up properly, the controller won't leave to serve a phase unless there's time for that phase to "meet its force off obligation". By definition, if the permitted phase is going to make it's force off obligation, then all successive phases must as well--there is no danger of a late return to the coordinated phase(s).

2. Permissives are automatically extended from the time that the coordinated green de-activates to the start of any non-coordinated green to insure phase service. In the case of CNA coordinated phases, the permissives will be extended from the end of WALK. Thus, the coordinated phase, which rests in walk, advances to PED CLEARANCE upon registration of a serviceable call when a permissive is active. The LMD will automatically extend the permissive during PED CLEARANCE until the green of the phase in question begins. Without this type of operation, the permissive would often end during PED CLEARANCE, re-apply omits, and the phase would not be serviced.

No "extra" service is offered to the phase because the omits will be re-applied if the permissive **ends while still in Walk** (i.e. no call came in). Presumably, if the permissives are programmed correctly, the phase should be extended service if the call arrives before the normal end of permissive. The automatic extension basically extends the permissive through PED CLEARANCE.

3. Although permissive periods have no effect on controller operation once the green of a non-coordinated phase begins, permissive 1-8 activity will be shown on the coordination timing run mode display.

FORCE OFFS

Force offs (1-8) are phase assignable. The force-off function causes the controller unit to terminate right of way on the programmed phase(s). The LMD coordinator will

maintain the force-off until the green terminates. Coordinated and non-coordinated phases may have assigned force offs. Timing is on a per cycle, per split basis. There are two keyboard selectable modes of force off operation in the LMD, as follows:

Fixed force offs. Each force off time is programmed as a fixed point in the cycle length. At the *assigned point* within the cycle, the force off will be activated if and only if the associated phase is active as determined by the phase associations and the corresponding phase green.

Floating force offs. Instead of fixed force offs, the force of values act more like *max times*, and begin timing with the associated phase green. Thus, when this mode is selected, each force off value is programmed as if it were a max (green) time rather than a fixed point in the cycle. Operationally, the difference is that an early starting non-coordinated phase (due to gap-outs or skipped phases) can get no more green time than allotted because the timer begins with green. Early starting non-coordinated phases *can* get more green in the fixed mode because they can extend up to their force off point. **Note that permissives** are the *only* parameters locking the phases to the background cycle in the floating force offs mode.

HOLD

Hold is applied to the coordinated phase(s) whenever the coordinated phase(s) is active and no permissive period is active. Hold will release when a permissive period activates.

OFFSET SEEKING MODES

The LMD coordinator will synchronize the background cycle zero point to the interconnect, FSK, or time based reference pulse, whichever is in effect. When in sync, the cycle zero point is offset from the master sync by a programmable value as determined by the active offset. The process of getting in sync with the master sync pulse is called "Offset Seeking". The LMD is capable of four selectable methods of offset seeking as follows:

a. Shortway offset seeking - In this method the unit will offset seek by varying the background cycle length, either shorter or longer, whichever direction most efficiently gets the unit in step. The background cycle length will not vary by more than 20% during the smoothing process.

b. Dwell offset seeking - In this method the unit will dwell at cycle zero until in step or until a programmable maximum dwell period is exceeded. One programmable maximum dwell period is provided for each cycle.

c. Interrupter mode - When in this mode and operating in an interconnect system with interrupter pulses, the unit will be capable of seeking, in dwell mode fashion, to the master sync pulse only and not to interrupter pulses. When in this mode and operating as a system master, the time clock offset outputs will issue 4 asynchronous (with the cycle) interrupter pulses per cycle in addition to the master sync pulse (see note 2)

d. Re-sync Mode - The re-sync mode is a manual cycle reset mode, executed on a one time basis. It is used to manually reset the current cycle on command, from which point it will free-run until power interruption. The re-sync mode is a temporary means of establishing coordination since power interruption discontinues re-sync operation. Offset sync pulses are ignored during re-sync operation.

NOTE 1

In general, offset seeking refers to the method in which the background cycle gets in step with the master sync pulse. Keep in mind that these are really two separate timers--even though they are the same value. The master cycle and corresponding sync pulse, regardless of source, is issued simultaneously to each unit in the system and is thus the system reference. The background cycle, is equivalent to the local cycle and may be offset from the master sync by a programmed value. Offset seeking is the process by which the local cycle achieves this offset (the re-sync mode manually resets the current local cycle).

NOTE 2

Offset seeking methods generally condition the internal background cycle. The cycle, split, and offset outputs, which would be used to drive an interconnect, are only affected by the interrupter mode which issues four asynchronous interrupter pulses per cycle in addition to the master sync pulse [(cycle- 2)/4]. In both other modes, the output sync pulses are unaffected by offset seeking and simply issue sync pulses once per cycle. It is up to the controller(s) receiving these pulses to get in step.

For those not familiar with interrupter pulses....

Interrupter pulses are most often used with electro-mechanical controller units. If an electromechanical controller arrives at its reset key late (i.e. the sync pulse has come and gone), it will dwell until the next sync pulse arrives. With a single pulse per cycle, this could be almost the entire cycle length. Since the dial is dwelling (stopped) for this entire period, the controller remains in its current interval (usually main street green) for this entire period. In many cases this is unacceptable. Interrupter pulses are simply 4 evenly spaced pulses issued in addition to the master sync pulse.

Since any pulse can release the dial, the controller will dwell no longer than the interval between interrupter pulses. Thus, the total required dwell is essentially spread over several cycles, each cycle getting closer to being in step. The interrupter pulses are based on a

slightly different cycle than the master cycle (2 seconds less divided by 4) so that the dial will never "sync in" on interrupter pulses.

Loss of sync pulses to free operation

The LMD is programmable such that it may remain in system operation upon loss of sync pulses (loss of sync pulses to free disabled) or will go free (loss of sync pulses to free enabled). When loss of sync pulses to free is disabled, the LMD will time its own cycle based on the last received sync pulse.

System to Max II, CNA

The LMD can be programmed to automatically select Max II and/or CNA upon entry into system. When CNA is selected, CNA I will be selected when the primary coord phases are active, and CNA II will be selected when the ALT coord phases are active. Note that the functions are implemented only when the LMD is actually in system, after the cycle timer is timing, force off's are being issued, etc, not just call for system.

Service/Max plans During Coordination

The LMD allows use of specially assigned "service" and "max" plans with each cycle/split combination. Service plans allow up to 8 sets of basic controller timing (min grn, passage, walk, PCL) and recall status to be implemented by cycle and split. Max plans allow 8 sets of phase max's to be implemented by cycle and split.

Free Operation

The LMD controller will automatically revert to free operation under any of the following conditions:

(1) If there is no call for system, either externally (AC input), through FSK communications, or via time clock (depending on which mode is in effect).

(2) If a particular cycle, split, and offset, designated as the "C/S/O to free" combination, is active.

(3) If free operation is manually selected through the keyboard.

(4) If the system override input is grounded (Lo = free).

(5) If pre-emption, Manual Control Enable (MCE), or Remote Flash is in effect.

(6) If the LMD is programmed for FSK communications (closed loop) and communications fails–but there is no clock command calling for system (note that clock is the back-up mode to FSK communications).

(7) If the LMD is programmed for "loss of sync pulse to free" enabled and sync pulses are not being received.

Interconnect Secondary Operation

The LMD has AC interconnect inputs on MSD capable of accepting a standard hardwire interconnect. The LMD can respond to standard or interrupter type sync pulses on the offset lines. If receiving interrupter pulses, the LMD must be in the interrupter mode.

Master operation (using time clock outputs)

The LMD can operate as a master, driving a hardwire interconnect. Master operation in the LMD is by use of the time clock coordination outputs. Selection of the cycle split and offset is by assignment of cycle/split/offset to time clock day programs, day programs to week programs, etc. Sync pulses are provided on the active time clock offset line, based on the offset selected and the sync reference mode in effect. The LMD, operating as a master, will respond internally to the same commands being issued on the interconnect (selected in the time clock mode).

Four Interrupter pulses will also be provided in addition to the master sync pulse *if the interrupter mode* is selected. These are based on (cycle - 2)/4.

Time Base Coordination

The LMD controller unit is capable of coordinated operation in response to internally generated time clock commands selecting cycle, split, and offset. In this mode the LMD coordinates with other time base units, without need of interconnect. There are four choices of sync reference modes available in the LMD (see sync reference definition). All units to be coordinated in one system must use the same reference mode.

Telemetry

The LMD can be expanded to accept TDM FSK type communications by insertion of a communications module. When so equipped, the LMD is capable of accepting coordination commands from a remote master.

ADAPTIVE SPLIT OPERATION

The Adaptive Split feature allows each intersection the capability of dynamically selecting its own split based on vehicular demand. Each split is assigned a set of selective phases. These are phases that apply to the selection of that split. The total number of force off's or Queues is determined for each split over the sample number of cycles. For example, say the force off mode is used, and split 2's selective phases are 3 and 7. Now, say that over the sample number of cycles, 3 forced off once and 7 forced off twice. The total for split 2 would then be 3.

Starting from split 1, the split with the **highest total exceeding the minimum threshold** is selected for the duration of the next sampling period. The LMD **will remain in the selected split until a new split with a higher number of force offs or Q's exceeding threshold occurs.** If two splits have the same number of F.O.'s or Q's, then the lower numbered split will be selected. For **semi-actuated** applications, **assign 0's to split 1** and let other splits be selected based on *exceeding the threshold*. The LMD will **default to split 1** if not exceeded in this mode.

If used, queues are based on the Q detector programming. Each phase is assigned up to 2 Q detectors (1-24) with delay periods. The delay timer times down when the detector is active, and sets to full value when inactive. If the detector is **active for the entire** delay period, a queue is registered for that phase. **Detectors 1-24 can be used as queue detectors.** Normal calls, extensions, or standard detector stretch and delay timing are not affected.

CSO TO CIRCUIT MAPPING

Any of the available Time Clock Circuits can be activated by selected combinations of cycle, split, offset, and/or system. Specify desired C/S/O with system/no system along with any time clock circuits to be active.

SCM (Subordinated Coordination Mode)

The LMD will tolerate phase "non-forcible over-timing by re-adjusting the cycle timer to the phases. This prevents skipping or short timing subsequent phases. Over-timing (phase unable to force-off when its supposed to) can occur for a number of reasons, often due to actuated peds that are seldomly used and thus do not warrant normal split timing. When over-timing occurs, the cycle timer will be out of sync, but will re-sync smoothly by normal offset seeking.

PRE-EMPTION FEATURES

The LMD Controller provides keyboard programmable pre-emption capable of up to six distinct sequences.

Pre-empt Timing Intervals

Preemption interval timing ranges are programmable from 0 - 9.9 seconds in .1 second increments or 0 - 127 seconds in 1 second increments.

Pre-emptor type

It is possible to program each of the 6 sequences as a "hold only" pre-emptor or as a "sequence" pre-emptor. The "hold only" pre-emptors are restricted to holding a phase green, if already green, for a settable duration. Sequence pre-emptors provide the ability to pre-empt from other phases and follow a defined sequence.

Minimum pre-empt re-service time

A minimum re-service time for each sequence is provided, making it possible to restrict the occurrence of the same pre-emption twice successively. This time is programmable in the LMD by the user on a per input basis from 0-99 minutes.

Priority/Remote Flash override

A priority level is assigned to each of the pre-empt inputs. Higher priority sequences will override and take precedence over lower priority sequences. Those of the same priority will be on a first come, first serve basis.

Each input also has the capability of overriding or not overriding remote flash (MSA Test A, DC Flash input, or Clock CKT 8 command). When overriding, the LMD will exit into the remote flash exit phases, then proceed to pre-emption.

Pre-empt Operation, Sequence type

When pre-empted, sequence type pre-emptors will proceed to the phases specified by the initial pre-emption interval. It is possible to pre-empt to a phase, a phase pair, or an all red condition. From this point the pre-empt sequence determines the subsequent phasing sequence. Each pre-empt interval can select a specific phase or phases, time the green duration and/or hold on input, turn any signal indication on or off, flash any signal indication, and/or turn on/off any of the pre-empt outputs.

Sequence type pre-emptors are capable of a pulse initiated timed sequence or a input duration sequence. When pre-empted, the LMD operates as follows:

If in yellow or all red *of any non pre-empt entry phase*, the LMD will continue the clearance intervals until completion, thereafter proceeding directly to the pre-empt entry interval phase(s) without regard to the "this phase next decision" (see pre-empt overlap description).

If in yellow or all red *of the pre-empt entry phase*, the LMD will continue clearance intervals until completion followed by the controller "Red Revert" setting. The unit shall proceed from this point directly to the pre-empt entry phase in the same manner as described previously.

If in green *of any non pre-empt entry phase*, the LMD will complete basic minimum timings prior to clearing the phase. These minimum timings are programmable on a per input basis and are specifically dedicated to entry into the pre-empt sequence when that input is ac-

activated. They override normal controller settings during entry into pre-emption only. These special timings include:

Pre-empt Minimum Green
Pre-empt Walk
Pre-empt Pedestrian Clearance

Overlaps During Pre-emption

Each overlap may individually be inhibited during the pre-empt sequence. If any overlaps require clearing due to inhibiting or because the controller overrides a "this phase next" decision (where the overlap is still green but needs to be cleared), the LMD will clear them prior to activation of the pre-empt entry phases. Clearance timings are obtained from special programmable timings provided for that purpose. These Include overlap Yellow and All Red.

Delay before pre-emption

The LMD provides a programmable a delay before pre-emption for each input, where delay is from the time the pre-empt input is asserted to implementation of the pre-empt plan (0 delay = immediate pre-empt). As an option, the controller can be programmed to omit all non-pre-empt entry phases and or all peds during the "Last X" seconds of the delay before pre-emption period (x is programmable). When this feature is not enabled, the LMD will operate normally until the delay before pre-empt period times out.

Pre-empt Input Memory ON/OFF

Each pre-emption input can be programmed to operate as a memory on or off input. When programmed memory off and there is a non-zero delay before pre-empt period, termination of the pre-empt input prior to the delay period will not initiate pre-empt operation.

Pre-empt Inputs and Outputs

Six pre-empt inputs (ground true) are provided for selection of one of the desired pre-emption plans. Up to six pre-empt outputs are also provided which are activated (ground true) when called for by the pre-empt sequence. Inputs are prioritized (see priority).

Coordination and Sync pulses during pre-emption

Internal coordination is suspended during pre-emption however, when the controller unit is used as a master, generation of external sync pulses is not affected.

Priority Return Pre-empt

Allows pre-empt to immediately return to a specific phase or phase pair if such phases were short timed upon pre-empt activation. The return operation is based on user definable thresholds.

TRANSIT PRIORITY

Transit priority is a "softer" form of prioritized service than pre-emption. In response to special inputs (I/O mapped) a transit vehicle can receive early service or extend beyond normal phase time, but not as aggressively as pre-emption typically would. The operation is intended for use in coordinated systems with special features included to control the impact on cycle timing and to recover coordination quickly and smoothly.

NEMA INPUT/OUTPUT DEFINITIONS

The following definitions relate to the NEMA defined functions. Functions which are not NEMA specified will be identified.

Standard TS-2 TYPE II I/O configurations

In the TYPE II version of the LMD9000 controller, eight user selectable (by three mode select pins) MSA, MSB, and MSC connector configurations are defined in addition to the TS-1 compatible version. These variations, in general, eliminate seldomly used or unassigned (by TS-1) pins and replace them with more current functions such as additional detector inputs, pre-empt, coordination, and/or time clock outputs.

If CUSTOM I/O MAPPING is disabled, which it is by default, the I/O mode is selected by the logic combination of the three I/O MODE PINS. I/O modes are selected by jumpers on the back-panel, low (0 VDC) = ON or active.

If it is necessary that custom I/O be utilized, the I/O MODE pins will be disregarded, and inputs and outputs will be custom programmed.

The three mode select pins are located on MSA and are labeled I/O mode bit A (pin q), I/O mode B (pin y), and I/O mode bit C (pin HH).

For example, if a cabinet were to be installed in system utilizing FSK communications for closed loop system operation, the back-panel would be wired to provide the MODE 2 (system interface) inputs to the controller.

The combination of the logic level of these pins defines the I/O configuration as follows:

	BIT			
MODE	A	B	C	STATE
0	off	off	off	TS-1
1	on	off	off	Hardwire interconnect
2	off	on	off	System interface
3	on	on	off	Reserved *
4	off	off	on	Reserved *
5	on	off	on	Reserved *
6	off	on	on	Manufacturer specific *
7	on	on	on	Manufacturer specific *

* Presently modes 3-7 disable all I/O mode dependent inputs and outputs.

Mode Dependent Inputs and outputs

There are 24 I/O mode dependent inputs and 24 I/O Mode dependent outputs (see "I/O mode select" pins above). The inputs are the former PHASE HOLD, PHASE OMIT, and PED OMIT. The outputs are the former PHASE CHECK, PHASE NEXT, and PHASE ON. See I/O Pin List for the different modes. Mode dependent inputs and outputs are labeled as Mode inputs 1-24 and Mode outputs 1-24, rather than their functions, in the pin list.

NEW (TS-2 Type 2) Inputs

There are also ten "new pins" previously not used on TS-1 controllers, these pins are NOT mode dependent (they are the same for all I/O modes). They are:

I/O mode Select pin (bit) A
I/O mode Select pin (bit) B
I/O mode Select pin (bit) C
Call to free *
Test C input
Pre-empt input 3 *
Pre-empt input 4 *
Pre-empt input 5 *
Pre-empt input 6 *
Indicator Lamp Control

* these inputs are also assigned to MSD pins, if so equipped.

EXTERNAL INPUT MODIFIERS

External inputs, when active, modify the normal operation of the controller unit in a pre-determined manner. Some of these inputs are provided on a "per phase" basis while other inputs are provided on a "per ring" or "per unit" basis. Note that in the following descriptions the terms "activation" or "applying" the input means grounding it (0 VDC), while "de-activation" means removing ground (24 VDC).

PER PHASE INPUT MODIFIERS

The following inputs are on a per phase basis, indicating there is one per each phase (1-8).

VEHICLE DETECTOR INPUTS

Provides means for input of call information from detector amplifiers. Operates in one of two user selected modes:

Memory on. Call is remembered until phase served, even if detector just pulses. Memory is cleared at the end of green, i.e. calls arriving during yellow and red are stored in memory.

Memory off. Detector input must be active at time of previous phase TØN decision. Used for right turns, etc.

The phase detectors can be optionally programmed for assignment to any phase. The detectors may also be programmed for stretch and delay features. The stretch feature extends the input actuation by a settable amount. The delay feature provides a delay period between the activation of the input and the actual registration of the call. The input must remain continuously active (LO) dur-

ing the entire delay timing period for a call to be registered. If the vehicle leaves the detector zone, and the detector amplifier contact opens before timing out, the timer will be reset and no call will be placed. Detectors would normally be used in the presence mode during delay detector operation.

PED DETECTOR INPUTS

Provides means for input of PED call. Ped call is always in the memory on mode.

HOLD

The HOLD function is a basic coordination function. Hold results in different controller response depending upon whether the phase is in the actuated or "call-to-non-actuated mode" (CNA).

1. Non-Actuated Phase (CNA). Activation of the HOLD input maintains the controller unit in the timed-out Walk period with GREEN and WALK indications displayed. Applying HOLD during walk does not inhibit the timing of walk. Reapplication of HOLD while timing ped clearance does not inhibit either the timing of this interval or the termination of the phase.

Deactivation of the HOLD input allows the controller unit to advance into ped clearance without regard to the presence of a serviceable conflicting call. However, if there is no serviceable conflicting call, the controller will rest in GREEN/DON'T WALK upon completion of ped clearance timing. If there is a serviceable conflicting call, the controller unit will advance to yellow change (see Walk Rest Modifier definition).

2. Actuated Phase. Activation of the HOLD input allows the controller unit to time normally but causes the controller to rest in GREEN/DON'T WALK after completion of ped clearance (if timed). Continued activation of the HOLD input inhibits the recycle of pedestrian service unless the PED CYCLE input is active.

Deactivation of the HOLD input with all intervals timed out will allow the controller unit to recycle the WALK interval if no serviceable conflicting call exists and a pedestrian call is stored on that phase. However, if there is a serviceable conflicting call with all intervals timed out, release of HOLD will cause the controller unit to advance into yellow change and will not recycle the WALK interval until it returns to the phase.

PHASE OMIT

The PHASE OMIT input causes omission of a phase from the phase sequence even in presence of demand. It inhibits its selection of the phase and continues in effect until the input is de-energized. The phase omitted does not present a conflicting call to any other phase but will accept and store calls. Phase omit does not inhibit service of a phase if a "this phase next" decision has been made and the controller is committed to service the phase. Phase omit does not cause termination or effect timing of a phase if applied during the phase (i.e. phase omit only has an effect if applied during the green of another phase).

PEDESTRIAN OMIT

The PED OMIT input inhibits the selection of a phase due to the presence of a pedestrian call on that phase and prohibits the servicing of a pedestrian call on the phase even though the phase may be serviced in response to a vehicle call. Activation of the input does not affect a pedestrian service in the process of timing at the time of its application.

PER RING INPUT MODIFIERS

The following modifiers are on a per ring basis, i.e. there is one each for ring 1 and ring 2.

FORCE-OFF

The FORCE-OFF causes termination of the GREEN timing and/or WALK- HOLD* if there is a serviceable conflicting call. The force-off function is not effective during the timing of Minimum green, Walk, or Ped Clearance. Force-off will override hold when both are applied. An automatic vehicle call is placed on the phase when it is terminated by force-off before the passage timer times out. The force-off input is effective only as long as the input is maintained.

*STATE B of a non-actuated phase

STOP TIMING

This input causes cessation of all timing within the related timing ring for the duration of the activation. When stop timing is deactivated, the interval timers will resume timing at the point of interruption. While stop timing is in effect, vehicle actuations will be registered on non-green phases and will reset the passage timer on a green phase. The controller unit will not terminate any interval or interval portion and it will not select another phase unless a complete operation of the Interval Advance input occurs (On/Off).

RED REST

This input results in REST-IN-RED operation of all phases in the related timing ring. That is, in absence of demand, the controller will return to ALL RED instead of resting in green of the last serviced phase. Registration of a serviceable conflicting call results in an immediate advance from RED REST to green of the demanding phase. Registration of a serviceable conflicting call before entry into the

RED REST state, even with this input active, will result in termination of the active phase and selection of the next phase in normal manner and with appropriate clearances.

A provision in the form of a keyboard data entry called RED REVERT insures that when RED REST is used and a call is received on the terminating phase without a serviceable conflicting call, a minimum selectable RED indication will be timed following the yellow interval and prior to the next display of GREEN on the same phase (i.e., green-yel-red-green indications on the same phase).

INHIBIT MAX TERMINATION

This input disables the maximum termination of phases in the related timing ring. Thus, the related phase may continue green indefinitely–as long as it receives detector extensions. The input does not inhibit the timing of the max timer, which starts in response to a serviceable conflicting call. It will time normally and is ready to terminate the GREEN if the inhibit max input is deactivated. Inhibit Max is often used during coordination whereby other means are provided to force off phases without interference.

OMIT RED CLEARANCE

This input causes omission of Red Clearance interval timing on all phases in the related timing ring even though Red Clearance time has been programmed. From LMD rev 7 upward, if the input is activated during the timing of a red clearance interval, it will clear the timer (not pre-rev 7).

MAX II SELECT

The MAX II SELECTION input allows selection of a second maximum time setting on all phases of the related timing ring, beginning at the start of the next green interval. Deactivation of this input results in the MAX I time setting.

PEDESTRIAN RECYCLE

This input is designed to control the recycling of the pedestrian movement. The response of the controller unit is dependent on whether the phase is operating in the actuated or non-actuated mode.

1. **ACTUATED MODE.** If a serviceable pedestrian call exists on the phase and the HOLD input is active, the pedestrian movement will be recycled when the Pedestrian Recycle input is active regardless of whether a serviceable conflicting call exists.

2. **NON-ACTUATED MODE.** If the phase has reached the Green/Dwell/Select state (STATE D), the PED OMIT input is not active on the phase, and a serviceable conflicting call does not exist, the pedestrian movement will be recycled when the Pedestrian Recycle input is on.

NOTE: The term "pedestrian recycle" is understood to be any start of pedestrian service after the start of phase green; i.e. a late ped service start or a 2nd ped service.

PER UNIT INPUT MODIFIERS

The following inputs are on a one per unit basis.

ALTERNATE SEQUENCES A-D (LEAD/LAG OPERATION)

Alternate Sequences make it possible to reverse the phase sequence on a phase pair basis. The phase pairs are 1-2, 3-4, 5-6, 7-8. When reversed, the odd phase will lag the even phase instead of leading it as is normal. Any combination of the phase pairs may be reversed. Since there are 4 pairs and each can be reversed or not, there is a total of 16 sequences available. The sequence selection may be made by activation of four input s(ASQ A-D), associated with a certain combination of cycle/split, or Timing Plan.

The alternate sequences are capable of:

AS-A - Phases 1 & 2 reversed
AS-B - Phases 3 & 4 reversed
AS-C - Phases 5 & 6 reversed
AS-D - Phases 7 & 8 reversed

Alternate Sequence inputs are interpreted as command requests as in the following table:

COMMAND INPUT	AS-A input	AS-B input	AS-C input	AS-D input
SEQ. 00	OFF	OFF	OFF	OFF
SEQ. 01	ON	OFF	OFF	OFF
SEQ. 02	OFF	ON	OFF	OFF
SEQ. 03	ON	ON	OFF	OFF
SEQ. 04	OFF	OFF	ON	OFF
SEQ. 05	ON	OFF	ON	OFF
SEQ. 06	OFF	ON	ON	OFF
SEQ. 07	ON	ON	ON	OFF
SEQ. 08	OFF	OFF	OFF	ON
SEQ. 09	ON	OFF	OFF	ON
SEQ. 10	OFF	ON	OFF	ON
SEQ. 11	ON	ON	OFF	ON
SEQ. 12	OFF	OFF	ON	ON
SEQ. 13	ON	OFF	ON	ON
SEQ. 14	OFF	ON	ON	ON
SEQ. 15	ON	ON	ON	ON

CALL TO CLOCK

This circuit forces time clock control for all operating parameters, regardless of their normal programming, i.e.; Comm, interconnect, etc.

CALL TO FREE (System override)

Activation of this input (Lo) causes immediate suspension of system operation. Typically used with a "system/free" external switch, or other external device.

CALL TO NON-ACTUATED I and II

Activation of either input places a permanent demand for vehicle and pedestrian service in associated phase(s). Associated phases are user programmable through the front panel keyboard. The resulting non-actuated phase(s) will be observed to consist of the following four (4) GREEN states:

STATE A	CODE 0*	WALK
STATE B	CODE 1	HOLD
STATE C	CODE 2	PED CLEAR
STATE D	CODE 3	GREEN REST

*Coded Status Bits Code

(a) State A is the minimum timing state. It is determined by the Walk interval time setting. Signal indications for the duration of State A are Green and Walk.

(b) State B immediately follow State A. The controller unit will be observed to dwell in State B as long as the Hold input is active and signal indications will continue to display GREEN and WALK on the phase. The controller unit will terminate State B, advancing the State C when the HOLD is released; or with the Hold input active and the Force-off input is activated but only if a serviceable conflicting call exists. However, if the Hold is released, the advance into State C will occur regardless of the presence of a serviceable conflicting call.

(c) State C is the Ped Clearance timing state. It is determined by the PED Clearance interval time setting. For the duration of this state, the controller unit will flash its DON'T WALK driver output while its Ped Clearance driver output is at GROUND. Reapplication of Hold during State C does not inhibit the Ped Clearance timing and resultant advance into State D upon completion of Ped Clearance timing.

(d) State D is the Green Rest or Green Dwell Select state. It is the state from which the controller unit selects the next phase to be serviced. The signal indications for the phase are Green and steady DON'T WALK. When a serviceable conflicting call does not exist and the PED RECYCLE input is active, the phase can return to State A and re-time the WALK interval. If the Ped Recycle input is not active, the pedestrian service cannot recycle even if no serviceable conflicting call exists.

The use of HOLD, FORCE-OFF, and PED RECYCLE inputs as described under States A - D inclusive suggest application of a semi-actuated controller in a coordinated system. The response and use of these inputs (which incidentally can be supplemented as need by the PED OMIT function) is clearly indicated.

The duration of the GREEN interval will be no less than the setting of the Minimum Green. In those instances when the sum of the Walk setting, the Hold state duration, and the Ped Clearance setting is less than the setting of the Minimum Green control, the controller unit will remain in State C until the phase has timed the Minimum Green setting. During this "waiting time", the pedestrian signal will display a steady DON'T WALK indication. There is thus a delay of the TØN decision until the Minimum Green and all other timing is complete.

CALL TO SYSTEM INPUT

Operational when "system" is programmed for the interconnect mode, or "AU" (coord modes, under coord menu) and interconnect inhibit is Hi. When operational and this input is activated, the controller is enabled to transfer from free operation to interconnect coordinated operation. The input would remain active for coordination to continue. Note that System Activation may also be determined by time clock circuit 13, or by FSK communications when not in the interconnect mode.

CALL TO WEEK PROGRAM 10

Activation of this input causes the LMD to immediately implement week program 10, regardless of the normal week program in effect as selected by the clock. The clock returns to the normal week program upon de-activation of the input (events are updated on input transitions--see week programs, in Time Clock section).

DIM (DIMMING CONTROL)

Use of this input allows selected signal outputs to be dimmed. Dimming consists of the controller half wave rectifying load switch circuit outputs through software control of the load switch inputs. Phase and color controller drivers can be keyboard programmed for positive half wave, negative half wave, or no dim allowed. Controller drivers operate normally when the dim input is not active.

DUAL ENTRY INPUT

When this input is grounded and the controller is operating in the dual ring mode, two phases will always be in service at any one time, one from each ring. Thus, if there is a call for service on one phase only, a call will be automatically placed on a compatible phase in the other ring. The phase association is loaded through the keyboard.

EXTERNAL MIN RECALL TO ALL VEHICLE PHASES

This input when activated places a minimum recall on all vehicle phases by registering a call in the vehicle memory while in YELLOW interval of the phase.

EXTERNAL START

Activation of this input causes the controller unit to immediately revert to its programmed initialization phase and interval. The controller unit will not begin timing the selected interval until the input is deactivated.

FLASH MONITOR 1 AND 2

This would be used to determine if the Terminals and Facilities (T/F) flasher AC output circuits are functional. AC flasher outputs are connected to these inputs. Flasher must drive AC off and on at approximately 1 hertz, if not, a failure could be logged.

INDICATOR LAMP CONTROL (TS-2)

This input has no function on the LMD9000 series controllers. However, it was intended to disable any controller unit front panel indicator lamps.

INTERCONNECT INHIBIT

Interconnect Inhibit may pertain to any of the following parameters; cycle, split, offset, flash and system--but only those that are programmed "Au" (auto) in the coordination manual/remote menu. For any programmed in this mode, interconnect inhibit will have an effect. When interconnect inhibit is Hi, any of these functions (programmed "AU") will be interconnect controlled, when Lo, any of these will be clock controlled (event programming).

INTERVAL ADVANCE

A complete on-off operation of this input will cause immediate termination of the interval in process of timing. It does not require operation in conjunction with STOP TIMING. When concurrent pedestrian timing exists, use of this input will cause first termination of the walk interval with continued green indication and a second operation will cause termination of the ped clearance interval and the green indication subject to presence of a serviceable conflicting call. Thus, in absence of a serviceable conflicting call, the controller unit will remain in a Green/Don't Walk state. Operation of Interval Advance (with or without Stop Timing active) will clear vehicle and/or ped calls stored in the phase when the controller unit is advanced through the green interval of that phase.

If a call for a pedestrian service does not exist, a complete operation of the interval advance input at any point in the green interval will cause the unit to advance to the Green Dwell/Select state from which it will immediately select the next phase and advance into the yellow interval subject to the presence of a serviceable conflicting call. In absence of a serviceable conflicting call, the controller unit will respond immediately to the registration of such call and advance to the yellow interval. If a vehicle passes over the detector on the green phase before a serviceable conflicting call is registered, the active phase will retain the green for at least one passage time.

I/O MODE INPUTS A-C

In the TYPE II version of the LMD9000 controller, eight user selectable (by three mode select pins) MSA, MSB, and MSC connector configurations are defined, in addition to the TS-1 compatible version. These variations, in general, eliminate seldomly used or unassigned (by TS-1) pins and replace them with more current functions such as additional detector inputs, pre-empt, coordination, and/or time clock outputs.

The combination of the logic level of these pins defines the I/O configuration as follows:

	BIT			
MODE	A	B	C	STATE
0	off	off	off	TS-1
1	on	off	off	Hardwire interconnect
2	off	on	off	System interface
3	on	on	off	Reserved *
4	off	off	on	Reserved *
5	on	off	on	Reserved *
6	off	on	on	Manufacturer specific *
7	on	on	on	Manufacturer specific *

* Presently modes 3-7 disable all I/O mode dependent inputs and outputs.

LOCAL FLASH STATUS

When this input is active, a time and date stamped message (LOCAL FLASH) will be stored in the controller's non-volatile memory. This is a status indicator only, activation of this input does not cause flash. This input would be driven by a cabinet door switch which would also activate the REMOTE FLASH (AUTOMATIC FLASH) input , causing flashing operation.

MANUAL CONTROL ENABLE

This input places vehicle and pedestrian calls on all phases, stops timing in all intervals except vehicle clearances, and inhibits the operation of Interval Advance during vehicle clearances. Vehicle clearance intervals (yellow and red) will be timed automatically by the controller unit. It is designed for use in conjunction with operation of the Interval Advance input. It must not be used with the STOP TIMING input active. Since vehicle and pedestrian calls are placed in all phases, two complete ON-OFF operations will be required to terminate the green (walk & ped clear).

MONITOR STATUS BITS A-C

Conflict monitor status bits A-C. The status bits from LSM or LNM monitors are interpreted and will be reported as "Conflict", "Red fail", etc. as follows:

BIT A	BIT C	BIT C	FAILURE MESSAGE
OFF	OFF	OFF	CONFLICT
ON	OFF	OFF	OVERLAPPING SIGNALS
OFF	ON	OFF	YELLOW CLEARANCE
ON	ON	OFF	WATCH DOG
OFF	OFF	ON	RED FAIL
ON	OFF	ON	+ 24 VDC FAIL
OFF	ON	ON	CVM FAIL
ON	ON	ON	NORMAL (OK)

MMU FLASH STATUS

When this input is active, a time and date stamped message (MMU FLASH) will be stored in the controller's non-volatile memory. This is a status indicator only, activation of this input does not cause flash. This input would be driven by an MMU output relay which closes during flashing conditions.

OFFSETS 1-3

When in the applicable mode, the controller unit will select the offset to be implemented based on the current status of the OFFSET request inputs. OFFSET inputs are interpreted as follows:

ACTIVE	Offset 1 input	Offset 2 input	Offset 3 input
Offset 1	ON	OFF	OFF
Offset 2	OFF	ON	OFF
Offset 3	OFF	OFF	OFF

PRE-EMPT 1-6 INPUTS

Each one of these inputs initiates one of 6 unique pre-empt sequences. Each pre-empt sequence is part of a customized internal software package created for the specific pre-empt application. This software will cause the controller to advance to the pre-empt phase(s) and initiate the pre-empt sequence pattern until the input is not active (see Pre-emption Section). In the case of a pulse signal, it will advance to the pre-empt sequence and time a settable duration. Each input can be operated in a memory on/off mode with settable delay before pre-empt.

REMOTE FLASH

When this input becomes active, a call for flash will be entered into the controller unit. The controller will then cycle to the phase(s) programmed as the entry phase(s), then proceeds to an all RED condition and transfers to flashing operation (CVM goes Hi). When the input becomes inactive, the controller will transfer from flashing operation back to automatic (CVM goes Lo) in the

phases and intervals programmed as the flash exit interval(s).

Note that there are two other ways to implement this same process, by AC remote flash (110 VAC active) and by time clock flash. The AC input requires connections to the MSD connector (with MSD I/O board inserted). Time clock flash and D.C. remote flash are available in the standard LMD.

SGO/CONDTIONAL SERVICE

Enables conditional service and simultaneous gap-out.

SYNC INHIBIT

When active, the time clock offset outputs are steady active when selected and do not pulse once per cycle.

SYSTEM ADDRESS SELECT INPUTS 0-4

Five system address select inputs are provided when I/O mode 2 is selected. The activity of these 5 inputs will define the ad-dress of the controller while operating in a system communications manner. As an alternative, system address may, and probably will, be defined controller software programming.

TEST A-C

These three inputs are provided for manufacturer specific use. The resulting function of these inputs is not defied by NEMA;

Test A – Activates REMOTE FLASH

Test B – Programming defines the test B input function; 0 = Enable dimming, 1=Call to free operation (disable coordination, often used with external comm units). 2=Call to free also but with an 180 second delay from initial activation to the return to internal coord. This prevents the LMD from attempting to return to internal coord after only a brief loss of comm at the RCU.

Test C - Undefined

TIME CLOCK RESYNC

Toggle low, then high resets the internal clock to a keyboard settable time of day on the rising edge of the pulse.

TIMING PLAN A-D

When in the applicable mode, the controller unit will select the timing plan (pattern) to be implemented based on the current status of the TIMING PLAN and OFFSET request inputs.

Pattern inputs are interpreted as follows: References to Cycle/Split combinations have been provided for use in a traditional interconnect system.

Timing plan	TPA	TPB	TPC	TPD	Reference
TP 00	OFF	OFF	OFF	OFF	C1S1
TP 01	OFF	OFF	ON	OFF	C1S2
TP 02	OFF	OFF	OFF	ON	C1S3
TP 03	OFF	OFF	ON	ON	C1S4
TP 04	ON	OFF	OFF	OFF	C2S1
TP 05	ON	OFF	ON	OFF	C2S2
TP 06	ON	OFF	OFF	ON	C2S3
TP 07	ON	OFF	ON	ON	C2S4
TP 08	OFF	ON	OFF	OFF	C3S1
TP 09	OFF	ON	ON	OFF	C3S2
TP 10	OFF	ON	OFF	ON	C3S3
TP 11	OFF	ON	ON	ON	C3S4
TP 12	ON	ON	OFF	OFF	C4S1
TP 13	ON	ON	ON	OFF	C4S2
TP 14	ON	ON	OFF	ON	C4S3
TP 15	ON	ON	ON	ON	C4S4

USER DEFINED INPUTS

There are 8 DC user defined inputs for report logs. activation and de-activation of these inputs are logged by the LMD. The LMD can then report these log's to central via system software where the inputs are defied (e.g. "cabinet door open" – see Reports).

WALK REST MODIFIER

This input modifies the operation of a CNA phase only. When active, all CNA phases will remain in the timed out walk state in absence of a serviceable conflicting call without requiring hold to be active. The controller will recycle the pedestrian movement upon reaching the Green Dwell/Select state (state D) if no serviceable conflicting call. When not active, CNA phases will not remain in walk unless the hold input is active.

COORD PED RECYCLE (CPR) MODIFIER

CPR is a later addition to the coordination input set to modify the operation of coord phase ped recycle. Normally when ped recycle is on and there is no conflicting demand, the coord phase ped will recycle immediately after ped clearance. This tends to thwart any permissives that remain active. When CPR input = ON, the coord phase is forced to rest in Green/Don't Walk after ped clear and is allowed to recycle the ped *only after all permissives have ended.* Because the Coord Phases remain green/Don't Walk during permissive periods, CPR allows efficient response to conflicting demand. CPR is typically used with CNA coord phases with WRM = OFF, but can also be used with standard ped recall on coord phases. CPR is a mappable input accessed from the I/O section. One way to use it is to map the SYS output (e.g. 447) to the CPR input. CPR is then invoked whenever system operation is active.

INTERCONNECT INPUTS

Interconnect inputs have been provided for direct interface with a standard 110VAC type interconnects. Opto isolated AC receive circuitry in the controller receives and isolates the AC commands from the controller circuitry. These inputs would generally be used when operating as a secondary unit in an interconnected system. Note that response to these inputs is dependent upon the LMD9000 being in the "interconnect" mode. The interconnect mode can be directly selected by keyboard entry - interconnect inhibit off, or by "interconnect inhibit auto" with the Time Clock interconnect inhibit input inactive.

CAUTION: DO NOT CONFUSE THE INTER CONNECT AC LEVEL INPUTS WITH TIME CLOCK DC LEVEL COORDINATION OUTPUTS. APPLYING AC LEVELS TO DC OUTPUTS WILL CAUSE SEVERE DAMAGE TO THE CONTROLLER UNIT. INTERCONNECT INPUTS ARE CLEARLY IDENTIFIED BY CYC2 IN, SPLIT 2 IN, ETC. AND ARE RESIDENT ON MSA ONLY.

Remote Flash (AC LEVEL)

This input can be used to request flashing operation from the system master, a Police Door switch, an external clock*, or any other remote source. Note that in the controller programming the response to this input is programmed to occur during specific intervals to accomplish Uniform Code Flash. The Flash entry phase allows the beginning of flashing operation only at the end of that designated phase. The Flash Exit phase allows reentry into normal operation at the designated phase.

NOTE: This input does not condition flashing operation caused by the Conflict Monitor. The Conflict Monitor will cause immediate flashing operation if it detects a conflict, voltage failure, etc.

Cycle 2, 3, 5 and Split 2, 3 IN (AC Level)

When programmed for interconnect mode, these inputs provide selection of the cycle to be in effect in accordance with the tables below.

The transfer from one Cycle to another is restricted to the end of a designated interval. These intervals are recorded on the Signal Plan Chart under CYCLE or SPLIT XFER. If no interval is designated as the Transfer interval, the transfer can occur at the end of the current interval timing when the Cycle or Split select input(s) change.

Cycle Inputs Vs. Active Cycle in Effect

	ACTIVE CYCLE							
	C1	**C2**	**C3**	**C4**	**C5**	**C6**	**C7**	**C8**
C2 IN	0V	115V	0V	115V	0V	115V	0V	115V
C3 IN	0V	0V	115V	115V	0V	0V	115V	115V
C5 IN	0V	0V	0V	0V	115V	115V	115V	115V

Split Inputs Vs. Active Split in Effect

When programmed for interconnect mode, these inputs provide selection of the split to be in effect in accordance with the tables below.

	ACTIVE SPLIT			
	S 1	**S 2**	**S 3**	**S 4**
SPLIT2 IN	0 V	115 V	0 V	115 V
SPLIT3 IN	0 V	0 V	115 V	115 V

Offsets 1, 2, 3 IN (Offsets 4 and 5 not available on AC interconnect)

When programmed in the interconnect mode, the selection of one of these three inputs provides the offset in effect. This input is provided by a master with a 3-second sync signal during each cycle.

The transfer from one Offset to another can be accomplished in one of three ways -- Dwell, Shortway, or interrupter. See the Offset Seeking description for the explanation of these modes.

System Input

This input is operational when "System" is programmed for the interconnect mode, or AUTO (Coord modes, under Timing Data Menu) and interconnect inhibit is Hi. When operational and this input is activated, the controller is enable to transfer from free operation to interconnect coordinated operation. The input would remain active for coordination to continue. Note that system activation may also be determined by time clock circuit 13, or by FSK communications when not in interconnect mode.

Interconnect Common

This input provides the controller unit with a common or return reference line for its interconnected inputs and is isolated from chassis ground and AC neutral.

OUTPUTS

Some outputs are provided on a "per phase" basis while other inputs are provided on a "per ring" or "per unit" basis. Note that in the following descriptions the term "activates" or "turns on" means the output is at ground potential, capable of sinking 250 MA of current. Inactive or off means the output transistor is off and the output is pulled up to + 24 VDC through 10,000 ohms.

PER PHASE OUTPUTS

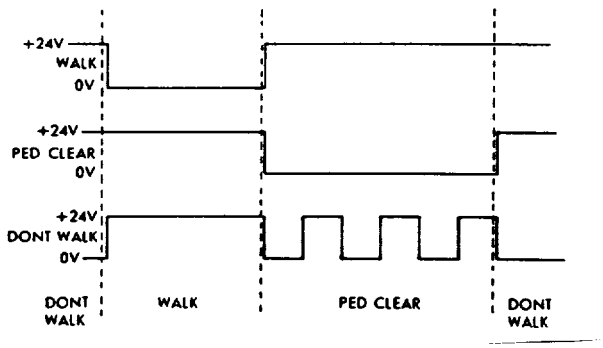
The following outputs are on a one per phase (1-8) basis.

VEHICLE LOAD SWITCH DRIVERS

Separate Green-Yellow-Red outputs are provided for each vehicle phase. A solid state circuit closure to LOGIC GROUND will be maintained at one of these outputs at all times. These outputs are used to energize the appropriate vehicle signal load switching circuit to result in a GREEN, YELLOW or RED indication for the duration of such required indication.

PEDESTRIAN LOAD SWITCH DRIVERS

Separate WALK/PED CLEARANCE/DON'T WALK outputs are provided for each phase. The DON'T WALK output is a steady output while FLASHING DON'T WALK flashes during the PED CLEARANCE interval.



When solid-state load switching is used for Ped signal control, the Ped Clearance driver output is not used. The Ped Clearance output enables use of relay load switching.

When the WALK is programmed in the Flash mode, the WALK output will flash to provide a flashing WALK indication.

CHECK

The CHECK output is used to indicate call status (vehicle or pedestrian) of the phase. This output is active when the controller unit is not in the green of that phase yet the phase has a demand for service stored in its vehicle or pedestrian memory or when operating in the MEMORY OFF mode as long as the detection zone is occupied. Neither the PHASE OMIT or the PED OMIT inputs have any effect on the CHECK output.

PHASE ON

This output is used to indicate phase status to external equipment such as external logic systems. The PHASE ON output of a particular phase is active (low state) during the green, yellow, or red clearance intervals of that phase.

PHASE NEXT (TØN)

An output of a phase activated when the phase is committed to be next in sequence and remains present until the phase becomes active. The phase next to be serviced is usually determined at the end of the green interval of the terminating phase. If the decision cannot be made at the end of the green interval it will be made at the end of the red clearance interval.

PER RING OUTPUTS

The following outputs are on a one each per ring basis (ring 1, ring 2).

CODED STATUS BITS

Three coded status bits per ring (R1 A,B,C; R2 A,B,C) provide external status of the basic controller timing intervals.

CODE	BIT A	BIT B	BIT C
0	+ 24	+ 24	+ 24
1	0	+ 24	+ 24
2	+ 24	0	+ 24
3	0	0	+ 24
4	+ 24	+ 24	0
5	0	+ 24	0
6	+ 24	0	0
7	0	0	0

The codes indicate the status of the controller as follows:

A. Actuated Controller, green interval.

Code 0: Minimum timing--Walk, Initial or Ped Clearance.

Code 1: Extension timing--After Initial, Walk and Ped Clearance have timed out, the controller is extending.

Code 2: Max timing--After minimum timing, when the Maximum timer is timing but not timing an extension (e.g. hold is applied).

Code 3: Green rest--After minimum, no passage timer timing, and the Max timer has timed out or has not started.

B. Non-Actuated mode, green interval.

Code 0: Walk Timing--Walk interval timing (non-actuated state A).

Code 1: Walk/Hold--When Walk output is active, Walk has timed out and hold input is active (non-actuated state B).

Code 2: Pedestrian Clearance timing--(non-actuated state C).

Code 3: Green rest--After Ped clearance and minimum timers have timed out (non actuated state D).

C. Actuated or Non-actuated mode, not in green interval.

Code 4: Yellow timing.

Code 5: Red clearance timing.

Code 6: Red Rest--Red clearance interval timing complete and Red output displayed.

Code 7: Pre-empt special Interval in effect.

PER UNIT OUTPUTS

The following outputs are provided on a "one per unit" basis.

Pre-empt 1-6

These outputs become active when set by the pre-empt instructions within the pre-emption sequence. They are also deactivated in the pre-empt sequence (see Pre-empt Section).

Flash Out

When remote flash has been called for, the all red interval has been timed, and CVM goes HI.

CONTROLLER VOLTAGE MONITOR (CVM)

An open collector output maintained low by the controller as long as the internally generated operating voltages are within specified tolerances. Used by the conflict monitor to place the controller in flash should voltages fail. Can also be driven by software to implement planned flash.

REGULATED + 24 VDC OUT

Provides regulated + 24VDC (+ /- 2VDC) over the AC line range of 95 VAC to 135 VAC, and from no load to full load. The capacity of this output is 500 milliamps continuous with less than .5 volts peak to peak ripple.

FLASHING LOGIC

Alternates between 0 VDC and + 24 VDC at a rate of 1 HZ with a 50% (+ /- 2%) duty cycle. This output is capable of sourcing (when at + 24 VDC) 50 milliamps of current and sinking (when at 0 VDC) 250 milliamps of current. The output will switch within 5 degrees of the zero crossover point of the AC line.

FAST FLASH LOGIC

(Canada only) This output provides an image of the fast flashing DC square wave of the signal to the conflict monitor or MMU. This signal provides the conflict monitor with the signal's flashing characteristics.

FAST FLASH STATUS

(Canada only) This is an output, used for Canadian Fast Flash operation. If any overlap is operated in the fast flash mode, fast flash active signifies that the unit is operating in that mode and fast flash image pulses at the same rate as the flash signal output.

ADVANCE WARNING

Advance warning consists of a per movement output that activates when the normal movement decides to terminate by gap-out, max-out, force-off, etc. The *actual termination* of the movement green is then delayed for a user definable period during which the advance warning output is active. The output remains active through yellow and red until the phase/overlap once again returns green and the Advance Warning De-activation Delay times out (ADD). The advance warning outputs are enabled when a phase as overlap or overlap has the AW feature ON.

FAULT MONITOR

This output is normally TRUE (low state) only as long as the voltages within the controller unit do not vary above or below pre-determined levels of voltage and quality required to maintain normal operation. This output can be used in place of CVM however, unlike CVM, this output will not go to the false state under non-fault flash conditions (i.e.; automatic flash, pre-empt flash, etc.).

SPECIAL FUNCTION 1-24 OUTPUTS

The LMD9000 is capable of issuing 24 special function bits. Special function bits 1-24 can be individually activated in any combination, by time clock command and/or special function commands from a system master (MDM100). These outputs will become active when any of the corresponding Special Function Commands become active (See Special Function Inputs).

DETECTOR SIMULATION OUTPUTS

Detector Simulation allows the controller to simulate detector calls. With this feature, the controller is capable of simulating an operating intersection. Calls are generated

based on a user defined SATURATION RATE (Vehicles per Hours, VPH) and a PERCENT OF SATURATION, the result of which is a TOTAL VOLUME. As an option, it is also possible to simulate speed (with a user definable pulse width) and waiting vehicle queue. Sixteen of the simulated detectors can be assigned to outputs to provide inputs to another controller or external device without detector simulation.

GENERAL COORDINATION OUTPUTS
The following outputs relate to coordinated operation - regardless of the mode (TBC, FSK comm, or Interconnect).

Circuit 13

This is the "system" (coord) output which is independently programmed. When system is in the clock mode and CKT 13 is on, a call for coordinated operation is in effect.

SYSTEM

This output becomes active after the system command becomes active and the first valid sync pulse has been received. The cycle timer with associated permissives and force offs will take effect. System output will remain on, even if sync pulses are not received, unless:

1. Sync pulses are lost and the LMD is programmed for “Loss of sync pulse to free” and thus goes free.
2. The call to free (system override) input is grounded.
3. The system command becomes Inactive.
4. The cycle, split, offset to free combination is active.
5. The unit is manually programmed for free operation.
6. The pre-emption, manual control enable, or remote flash inputs are activated.
7. There is a loss of FSK communications (if used) and there Is no back-up clock plan calling for system (clock is the back-up mode to FSK communications).

Note that depending on the mode (see time clock coordination outputs) system out (and coordination) can be determined manually, by Interconnect, FSK communications, or time clock circuit 13.

System out may be used to call for a specific function to be implemented during coordination such as INHIBIT MAX. Note that MAX II or CNA may be *Internally* programmed for system operation *without need* for external wiring. Either Inhibit Max (system out) or MAX II (internally programmed) are often implemented during coordination so that phases are terminated by force off’s, not max’s.

COORDINATION CLOCK CKTs 1-8,13

These clock circuit outputs are primarily used when the LMD is operating as a master, driving a hard wired interconnect. The controller will also internally respond to time clock coordination commands when these functions are programmed in the time clock mode and system (CKT 13) is called for.

Cycle 2,3 Out (Ckt 1,2)

Activity of these outputs is determined by time clock selection of Cycle. Activity of these outputs in relation to the selected cycle is as follows:

Coord Plan Cycle	CKT # 1	CKT # 2
Cycle 1 or 5	OFF	OFF
Cycle 2 or 6	ON	OFF
Cycle 3 or 7	OFF	ON
Cycle 4 or 8	ON	ON

Notes:

-When a new cycle is called for, the actual cycle output circuits immediately change states but the cycle timer finishes the current cycle before starting the new cycle.

-The cycle outputs follow the clock only or the general selection of cycle (regardless of mode), depending on the Coord Out setting (MM-2-4-2).

-Cycles 1-8 can be selected by CL master or TOD day plan. Cycles 1-4 only are selectable by interconnect.

Time clock Offset 1,2,3 Out

Activity of these outputs is determined by time clock programming, specifically the offset portion of the coordination plan (there are no offset 4, 5 outputs). Sync pulses are automatically issued once per cycle on the active offset based on the active cycle. When the interrupter mode is in effect, four interrupter pulses are issued in addition to the master sync pulse at a rate of (cycle length – 2)/4.

Note that offset outputs are equivalent to the master sync pulses and do not reflect the local offset. The local offset timing is internal to the controller. Thus, the beginning of the local cycle should be offset from the offset outputs by the offset value.

Split 2,3 Out (Ckt # 6, 7)

Activity of these outputs is determined by time clock programming, specifically the split portion of the coordination plan. Activity of these outputs in relation to the selected split is as follows:

Coord Plan Split	Ckt 6	Ck 7
Split 1	OFF	OFF
Split 2	ON	OFF
Split 3	OFF	ON
Split 4	ON	ON

Output Circuit 8 (Call for Remote Flash)

CKT 8 is the “Call for Flash” or “Remote Flash” function. Its effect on controller operation is determined by the mode it is programmed for (under coordination manual/remote programming). When in the clock mode, the controller will respond exactly as if the External Flash input had been activated. The unit will cycle to the Rash entry phase, clear to all red, then the CVM (Controller Voltage Monitor) output will go high (+ 24VDC). The monitor will then place the intersection in flash.

At this point, Flash out (see flash out description, pg 2-27) will go true (see Note 2), and the unit will enter flashing operation and remain there until the flash output is turned off (manually or by event programming). The unit will at this time return to normal operation in the interval specified by the Flash exit interval stored in EEPROM.

Notes:

1.**The controller will internally respond** to the Flash call circuit even without the system being called for—as long as the flash function Is programmed for clock (under coordination modes menu) or is programmed auto and interconnect inhibit is active.

2.The time clock “Flash Call” circuit output (CKT 8) is not the same as the “Flash Output”. The time clock flash command simply calls for flashing operation and initiates the sequence. The Flash Output becomes active when the controller actually reaches the flash entry point, regardless of the mode of selection, time clock, FSK, or input. This circuit could be used for any special requirements applied when the controller reaches the flash interval (All Red after entry phase).

Also note that Flash out is also pre-empt 6 out—do not use pre-empt 6 out if remote flash is used.

3. Remote flash can be overridden by pre-empt sequences- if programmed to do so. Also, preemption can programmed to provide “Soft Flash”, in which the load switch outputs provide flashing operation without dropping the flash transfer relays.

Output Circuits 9, 10, 11, 12

These outputs are general use outputs to be used as desired in accordance with time clock event programming, and/or manual programming. These outputs have no associated internal response.

MAPPABLE INPUTS AND OUTPUTS

A number of inputs and outputs have been added to the LMD since the inception of mappable I/O. Each time specific functions have been added, corresponding input and output functions have been added as well. It is then up to the user to decide what pin to use these on by substituting them for seldom used normal functions.

Some examples of such I/O are

Function	Parent Function	I or O
Pre-empt No delay	Pre-emption	I
Transit priority inputs	Transit Priority	I
AW outputs	Advanced warning	O
PE acknowledge	Pre-emption	O

External Harnesses

The list below identifies part numbers for interface cables. s/l = sliding locks used on TS-1 style applications, l/b = latching blocks used for TS-2 applications.

Harness for	Part Number
Modem, 9 pin (s/l)	0806149
Modem, 9 pin (l/b)	0807598
Comm Inputs, 15 pin (s/l)	0806148
Comm inputs, 15 pin (l/b)	0807597
Port 1 (SDLC)	0807605
LMD to LMD Data Xfer/Print (s/l)	0807252
LMD to LMD Data Xfer/Print (l/b)	0807295
PC up/download, 25 pin (s/l)	0807208
PC up/download, 25 pin (l/b)	0807596
PC up/download, 9 pin (s/l)	0807209
PC up/download, 9 pin (l/b)	TBA
Dial-up modem (s/l)	0806147
Dial-up modem (l/b)	TBA
LMD to LNME interface	0807375
Diagnostics	TBA
MSA	0804050
MSB	0804051
MSC	0804052
MSD w/PE, Aux outputs*	0807124-3
MSD w/PE, Interconnect	0807124-4
MSO w/PE, Coord Ckt’s 1-13	0807124-5
MSO w/PE, Aux out, det’s 9- 16	0807124-6
MSO w/Full harness, 5 feet	0807124-7
MSD w/Full harness, 9 feet	0807124-8
MSD w/PE Aux out, det's 9-16, DC user defined and special inputs	0807124-9

*Aux outputs = clock output Ckt’s 9-12.

SECTION III

DISPLAYS AND RUN MODE

INTRODUCTION

The LMD controller uses a menu driven display format for data entry and status information. The menu lists a number of choices from a group of major categories. Select a desired category by pressing the corresponding digit. There may be a sub-menu listing more choices. Continue the selection process until your specific segment appears.

POWER ON SELF TEST (POST)

Upon power-up, the LMD executes a self testing routine prior to activation of controller outputs and normal controller functions. The routine is about a second long and checks PROM, RAM, EEPROM, RTC (Real Time Clock), and I/O MODE. If these components are all normal, the test screen appears only briefly and the controller initializes normally.

```
      --POST (POWER ON SELF TEST)--
BATTERY-----GOOD    EEPROM------GOOD
PROM--------GOOD    RTC---------GOOD
RAM----128K-GOOD    MSA IO MODE-GOOD
```

To return to this screen hit Main Menu, Prior Menu twice.

If there is a failure, the test screen will freeze and a code will be displayed as shown below. The controller outputs at this point will become active, but *Controller Voltage Monitor* will not activate to the "good" state.

CODE	COMPONENT	CODE	COMPONENT
PROM			
1201	PROM U27	1203	PROM U28
1202	PROM U22	1204	PROM U23
RAM			
1301	RAM U29		
1302	RAM U24		
EEPROM			
1401	EEPROM U31	1403	DMA U16
1402	EEPROM U26		
RTC (REAL TIME CLOCK)			
1501	RTC U9		

MSA I/O Mode

Upon power-up, the controller will verify that the I/O (input/output) mode select inputs have not changed state since the last operational period, thereby reconfiguring the inputs and outputs. If different the follwing screen will appear at power-up. See I/O Section for more information.

```
CABINET CALLING FOR TS2 TYPE 2 MODE:0
CONTROLLER WAS IN MODE:2
HIT ENTER      TO ACCEPT NEW I/O MODE
HIT MAIN MENU TO CONTINUE IN FLASH
```

STANDARD DISPLAYS

If the LMD is fuctioning normally, the POST screen only appears briefly. The unit then increments to the initialization screen which indicates the revision level of the firmware.

```
_| |_ PROG 0807561 R 1A ACTUATED 19JAN94
_TCT_ COPYRIGHT 1993 ALL RIGHTS RESERVED
 | |  TRAFFIC CONTROL TECHNOLOGIES, INC.
INTERSECTION: MARKETPLACE AND 5TH ST.
```

Press the "MAIN MENU" key to get.....

```
            --MAIN MENU--
  1.RUN MODE              3.UTILITIES
  2.PROGRAM/READ MODE     4.I/O CONFIGURE
        --USE HELP KEY FOR HELP--
```

Hit Main Menu, Prior Menu to return to copyright screen

The "MAIN MENU" lists the 4 major display categories:

The Run mode provides real time status displays of controller operation, active phases and intervals, timers timing, vehicle actuation status, etc.

The Program/Read mode provides access to data entry and readout of all programmable functions within the unit. A security code may be loaded to prohibit data entry to unauthorized personnel.

The Utilities mode provides diagnostics as well as certain other data management and special functions such as copy backup timing, clear codes, controller restart, data print and transfer codes, and intersection naming.

The I/O Configure mode provides the ability to program the inputs and outputs in any of the TS-1, TS-2 and/or custom modes.

Note: The display backlight (if on) will automatically turn off after 10 minutes of keyboard inactivity.

RUN MODE

The run mode is used to observe the real time status of the controller unit. The LMD provides a variety of run mode screens to observe timing status, operational status, and input/output status.

There are two ways to access the Run Mode display:

1. From the main menu by selecting the RUN MODE and appropriate sub-menus.

2. Simply hit the "*Run Status*" pushbutton. This will cause the unit to immediately go into the basic run status display from any other display, run or program.

Once a run mode display is selected, others can be accessed by pressing the PGUP or PGDN keys or by returning to the prior menu and selecting a new display. When paging thru the displays, they will follow the same relative order as listed on the menu screens.

FUNCTION KEYS

RUN SCREEN 'HOT KEYS"

It is possible to program the most often used RUN MODE screens to correspond to the 0-9 keys on the front panel. To program, advance to one of the most used RUN MODE screens and press "." "1". Now anytime the "1" key is depressed, while in any RUN MODE screen, that screen will be displayed. Proceed to the next most often used screen and press "." "2" and any time "2" is pressed, that screen will be displayed. Program up to 10 (0-9) RUN MODE screens "hot keys".

To advance through the programmed screens, in order, depress the < ENTER> key from any RUN MODE screen. To delete a screen from the hot key programming, proceed to that screen and press "." followed by "CLEAR". That number is now free to be programmed as any other RUN MODE screen. When the "↑" is pressed, the following screen will be displayed.....

```
      --KEYS (0-9) AS FUNCTIONS--
<LFT ARROW=ENAB KEYS AS RUN SCRN SELECT
>RGT ARROW=ENAB KEYS AS VEHICLE 1-8 CALL
^ UP ARROW=SELECT NEW RIGHT ARROW MODE
```

ENTERING VEHICLE CALLS, PED CALLS, and PRE-EMPT CALLS FROM RUN STATUS SCREENS

To enter vehicle calls , pedestrian calls, or pre-empt calls using the keyboard, press "↑"

Vehicle Calls

Press "→" once and return to the RUN STATUS screen.....

Use the appropriate keyboard number (1-8) to enter vehicle calls to any or all phases.

Pedestrian Calls

Press "↑" twice (this changes VEHICLE CALLS to PED CALLS) and return to the RUN STATUS screen.....

Use the appropriate keyboard number (1-8) to enter pedestrian calls to any or all phases.

```
PHASE/OL 1:2 3 4 5:6 7 8 A B C D | CYCLE
SPD      r G r r r G r r r r r r | W XYZ
MIN XY   WLK XY |MIN XY   WLK XY | OFST
MXL XY   PSG XY |MXL XY   PSG XY | W XYZ
```

On the RUN STATUS screen active calls will be indicated by the presence of a "dot" preceding the phase number. The lower "dot" represents a vehicle call and the upper "dot" indicates the presence of a pedestrian call. In the above example, phase 2 has both a vehicle and a ped call present, while phase 6 has only a vehicle call.

Pre-empt Calls

Press "↑" three times and return to the RUN STATUS screen.....

Use the appropriate keyboard number (1-8) to enter pre-empt calls.

RUN MODE SCREENS

The following is a listing of run mode displays, starting from the main menu and proceeding through.

```
            --MAIN MENU--
1.RUN MODE              3.UTILITIES
2.PROGRAM/READ MODE     4.I/OCONFIGURE
      --USE HELP KEY FOR HELP--
```

Selection 1 ...RUN MODE

```
        --BASIC STATUS MENU--
1.RUN MENUS  4.PREEMPT       7.MMU STATUS
2.FAULTS     5.MOE/VOL/STAT  8.TRANSIT PR
3.CLOCK STAT 6.SCHED LOGS
```

BASIC STATUS RUN MODE DISPLAY

```
          --RUN MODE MENU--
1.BASIC STATUS 4.VOL/DENS 7.CODED STATUS
2.COORD TIMING 5.CLOCK    8.PH SERVICE
3.COORD STATUS 6.I/O STAT 9.COMM STATUS
```

Selection 1...BASIC STATUS...(this display is also accessed by pressing the "RUN STATUS" push-button)....

```
PHASE/OL 1 2 3 4 5 6 7 8 A B C D  CYCLE
SP0      r G r r r G r r r r r r  W XYZ
MIN XY   WLK XY  MIN XY    WLK XY  OFST
MX1 XY   PSG XY  MX1 XY    PSG XY  W XYZ
```

PHASE/OL.... Phases 1-8, overlap A,B,C,D. A decimal in front of phase 1-8 represents a vehicle actuation.

Below each phase, any of the following may appear:

R = Red (while other phases are in service)
R = Red Clearance (of that phase)
Y = Yellow
w = Walk
D = Don't Walk
G = Green
N = This Phase Next

SPO-8.....The active service plan 0-8 will be indicated here. SPO indicates that no service plan is in effect and the normal NEMA settings are in effect. SP1-8 indicates that a service plan 1-8 has been called by clock or CSO-see run mode display menu, *phase service display,* second page.

MIN XY.....Any of the following may appear:

MIN XY	=	Minimum Green timer timing
EXTD'G	=	Phase is extending
MAX REC	=	Phase is on Max recall
CNA 1 or 2	=	Phase is a CNA 1 or 2 phase

WLK XY.....Any of the following may appear:

WLK XY	=	Walk timer timing
DWXY	=	Don't Walk timer timing
WLK REST	=	Phase is in Walk Rest
GRN REST	=	Phase is in Green Rest
HOLD	=	The phase has hold applied
RED REST	=	Phase is Red Rest
STP TIME	=	Stop time applied in that ring
MCE	=	Manual Control Enabled
FRC OFF	=	Phase is being forced off
GAP OUT	=	Phase has gapped out
MAX OUT	=	Phase has Maxed out
VAR INIT	=	The initial has been lengthened (variable initial in effect)
SGO REST	=	The phase is resting in that ring due to "Simultaneous Gap Out Inhibit", i.e. it cannot restart its passage timer and is waiting to cross the barrier with the phase in the other ring. It is a subset of "GREEN REST".
CND SERV	=	The phase is being condition-ally re-serviced.
TPX	=	Transit priority phase is extending

MX1 XY.....Any of the following may appear:

MX2 XY	=	NEMA Max 2 timer timing (MAX 2 in effect)
MP1-8 XY	=	Max Plan 1-8 in effect (Clk, CSO)
MF1-8 XY	=	Max Fail Recall 1-8 due to detector failure
INH MAX	=	Inhibit Max in effect
TGX	=	Transit priority timing group used

PSG XY..... Any of the following may appear:

PSG XY = Passage Timer Timing
YEL XY = Yellow Timer Timing
RED XY = Red Timer Timing
TPR PHS = Transit priority phases active

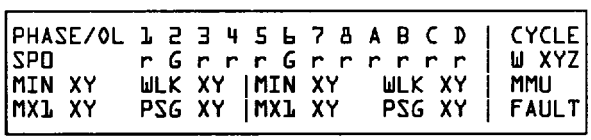
CYCLE..... The cycle in effect (local) and timer will be displayed.**"FREE OP"** will be displayed if the unit is not coordinating.

OFST..... The offset in effect and timer. **"SEEK"** will be displayed in place of **"OFST"** if the unit is currently offset seeking.

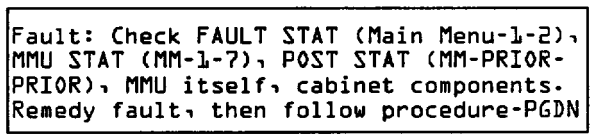
RUN SCREEN FAULTS

In the event of a cabinet failure, several different failures can be diplayed in the lower right hand corner on the RUN STATUS screen. In the event there is more than one fault, the display will toggle through all applicable messages until they are cleared. PRESS "HELP" and follow instructions to remedy. Also, see FAULT STATUS (press Main Menu, 1, 2), MMU STATUS (Main Menu 1, 7), and POWER ON SELF TEST (Main Menu, Prior Menu, Prior Menu) and read about these topics later in this chapter.

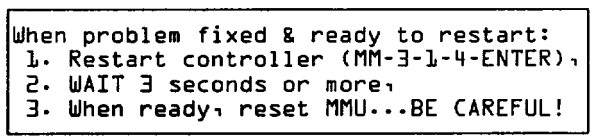
For example.....



If a fault has been detected, the type of fault will be display in the bottom right of screen. By pressing HELP the following screen will be displayed.....


Fault: Check FAULT STAT (Main Menu-1-2),
MMU STAT (MM-1-7), POST STAT (MM-PRIOR-
PRIOR), MMU itself, cabinet components.
Remedy fault, then follow procedure-PGDN

Page Down.....


When problem fixed & ready to restart:
1. Restart controller (MM-3-1-4-ENTER),
2. WAIT 3 seconds or more,
3. When ready, reset MMU...BE CAREFUL!

RUN SCREEN FAULT LIST

ControllerMMU Faults

The following three faults are generated by the controller as a result of controller/MMU errors:

CNTRLR COMPAT	The controller sequence is not compatible with the conflict monitor programming card jumpers.
CONTRLR CNFLCT	The controller has detected a conflict by comparing its sequence with the actual siganl outputs sensed by the MMU.
PORT 1 FAIL	The high speed communication channel between the controller and the MMU has failed to maintain communications.

Power On Self Test Faults

The following faults are a result of POST (Power On Self Test). Return to POST screen (press Main Menu-Prior Menu-Prior Menu) and see page 3-1 for failed component codes:

PROM CKSUM	The calculated Programmable Read-Only Memory Checksum value has changed since last power-up.
RAM FAIL	Random Access Memory has failed the Power On Self Test.
EEPROM FAIL	Electrical Erasable Programmable Read-only Memory has failed the Power On Self Test.
RTC FAIL	The Real Time Clock has failed the Power On Self Test.
IOMODE ERR	The Input/output mode inputs (on MSA) have changed state since the last power-up. (Upon power-up, a message will also appear with a warning of this condition). See page 3-1.

Checksum Faults

The following faults are a result of Checksum errors. Go to FAULT STATUS (press Main Menu, 1, 2) for description of fault and repair as necessary. Also see FAULT STATUS section later in this chapter.

CHKSUM LATCH	The controller is latched or forced into failure mode, which means the checksum failure must be cleared and the controller must be restarted to clear the latching condition.
CNTRLR CHKSUM	A checksum failure was detected in the controller programming area. Follow procedure in FAULT STATUS section later in this chapter.
COORD CHKSUM	A checksum failure was detected in the coordination programming area. Follow procedure in FAULT STATUS section later in this chapter.

(continued)

TIMCLK CHKSUM A checksum failure was detected in the time clock programming area. Follow procedure in FAULT STATUS section later in this chapter.

PREMPT CHKSUM A checksum failure was detected in the pre-empt programming area. Follow procedure in FAULT STATUS section later in this chapter.

IOMAP CHKSUM A checksum failure was detected in the input/output programming area. Follow procedure in FAULT STATUS section later in this chapter.

MMU Fault

The following fault is generated by the MMU and is a latched failure. See MMU STATUS (Main Menu 1, 7) and FAULT STATUS (press Main Menu, 1, 2).

MMU FAULT The MMU has detected a fault such as; conflict min clear fail, 24 VDC fail, Port 1 fail, etc.

COORDINATION TIMING DISPLAY

PG DWN OR PRIOR MENU...Selection 2...COORD TIMING

```
PHSE 1 2 3 4 5 6 7 8 | CYC 1 SPlT 1   0
IND. r W r r r W r r |  SEEK OFST 2   0
F.O.   2       6     | MASTER CYC 1  41
PERM 1       5       |HOLD |TBC 15:10:33
```

PHSE.....Phases 1-8

IND.....Active indications, where:

- r = Red when other phases are being serviced
- R = Red Clearance (of that phase)
- Y = Yellow
- W = Walk
- D = Don't Walk
- G = Green
- N = This Phase Next

F.O...... Force off's 1-8 will appear when activated

PERM..... Permissives 1-8 will appear when activated

CYC X SPLT XYZ.....Local cycle and split in effect and timer.

LOCAL OFST... The offset in effect and timer. "SEEK OFST" will be displayed if offset seeking.

MASTER CYC.. Master cycle in effect and timer.

HOLD.....Any of the following may be displayed:

- HOLD = The coordinated phase is in hold (no permissives are currently active).
- PEDP = The pedestrian permissive period is active

TBC.....Any of the following may be displayed:

- TBC HH:MM:SS = Time base coordination is in effect, With the time of day clock shown.
- INTERCONNECT = Interconnect Mode in Effect
- TELEMETRY = Telemetry mode in effect
- MIXED MODES = A combination of modes in effect.

COORDINATION MODE DISPLAY

PG DWN OR PRIOR MENU..Selection 3...COORD STATUS

```
       C/S/O | SYNC STAT: IN SYNC
MASTER:1 1 1 | CYC 1=  80 | OFST 1= 0
  MODE:C C C | SYNC REF: 8 INDEPENDENT
SYSTEM MODE: IN SYSTEM TBC MODE
```

MASTER..... Indicates active cycle, split, offset being called for.

MODE..... Indicates the mode of selection where:

- M= Manual T= Telemetry
- C= Clock (TBC) I = Interconnect
- L= Local split selection (adaptive split)

SYNC STAT.....Indicates coordination status:

- IN SYNC = Cycle timer is in step with sync pulse
- NOT IN SYNC = The local cycle timer is not in sync

CYC X..... Indicates cycle in effect and cycle length

OFST X..... Indicates offset in effect and offset value

SYNC REF.....Indicates type of sync reference mode;

- END OF PREV = End of previous cycle method
- 8 INDEPENDENT = 8 independent daily ref.
- ABSOLUTE = Absolute sync reference mode
- EVENT (CYCLE) = Referenced to the event time
- NOT IN TBC N/A = Offset sync pulses not TBC

SYSTEM MODE……Indicates system mode/status:

IN SYSTEM: INTERCONNECT MODE
IN SYSTEM: TBC MODE
IN SYSTEM: TBC, LOST CARRIER
IN SYSTEM: TELEMETRY
FREE: NO SYNC PULSE YET
FREE: LOST SYNC PULSE
FREE: COMB CSO TO FREE
FREE: TBC, LOST CARRIER
FREE: NO CALL FOR SYSTEM
FREE: MANUALLY PROGRAMMED
FREE: MANUAL CONTROL ACTIVE
FREE: FLASH COMMAND ACTIVE
FREE: PRE-EMPTION ACTIVE
FREE: CALL TO FREE, INPUT/CLOCK

VOLUME DENSITY STATUS DISPLAY

PG DWN OR.PRIOR MENU..Selection 4...VOL/DENS

```
PHASE 2  INIT  5    | PHASE 6   INIT  5
MAX   2  TBR   12   | MAXD  2   TBR   12
TTR   0  PSG   4    | TTR   0   PSG   4
CURRENT GAP    2    | CURRENT GAP     2
```

Left side is Ring 1, right side is ring 2.
PHASE X, Y…….Current phases ring 1 and 2
INIT XY……..…….. Initial green (min green) timing:
INIT XY = Nominal min green setting
VINIT XY = Variable Initial in effect
MAX XY……...Max timer timing
TBR XY……Time before reduction timer timing
TTR XY……Time to reduce timer timing
PSG XY……Passage timer timing
CURRENT GAP….Any of the following may appear:
CURRENT GAP XY = Current Value of passage
CNA MODE = Phase in CNA mode, gap is N/A
MAX REC = Phase in Recall Max, gap is N/A
PED TIMING = Phase in Ped timing, gap is N/A

TIME CLOCK EVENT STATUS

PG DWN OR…PRIOR MENU…Selection 5…

This section consists of two types of status; the first is the clock event status, which shows the time, date, service, and max plan called for, as well active clock CSO (see note). The second type of status shows the active state (on or off) of each the numerous clock circuits.

NOTE: Time clock circuit status screens can be found in sub-menu (8) under I/O status.

SELECTION 1….TIME CLOCK EVENT STATUS…...

```
TIME:  16:04:33     DATE:  08/14/90
WEEK |WK PROG|DAY |DY PRG |SP|MP|C/S/O
 22  |   1   |THU |   1   |1 |1 |1 1 1
                   MODE:  C  C  C C C
```

TIME, DATE……..Time of day, date of year displayed
Week 1-53…..…...Week of year displayed; 01 = week of Jan 1, etc.
WEEK PROG 1-10.Week program currently in effect
DAY WXY……..Day of week: MON, TUE, WED, etc.
DAY PRG 1-15….Day program currently in effect
SPO-8……Service Plan 0-8 (as called by clock)
MPO-8……Max Plan 0-8 (as called by clock)
C/S/O…….Clock event cycle, split, and offset.

Note: This is the Clock event cycle, split, offset selection and is the *actual* C/S/O in effect only if the *mode* is time clock or manual. The C/S/O indictions will match the manual mode selections when in the manual mode (manual overrides clock).

MODE XX XXX……Indicates the selection mode, where:

M=Manual
T= Telemetry
C= Clock (TBC)
I=Interconnect
L= Local Split Selection (adaptive split)
S= Cycle/Split

Note: The time clock event selections (directly above the mode indications) are the actual C/S/O in effect only if the mode is clock or manual.

I/O STATUS

This section provides active status of all LMD inputs and outputs in terms of the controller's perception of such status.

PG DWN..OR.PRIOR MENU...Selection 6…I/O Status

```
        --I/O STATUS DISPLAYS--
1.I/O MODES     4.RING/UNIT 7.TCLK CKTS
2.PHASE INPUTS  5.PREEMPT   8.INPUTS
3.PHASE OUTPTS  6.DETECTORS 9.OUTPUTS
```

I/O MODES DISPLAY

Selection 1.....I/O MODES.....

```
MMU DISABLE: |  I/O MODE: 0   |PEER POLL:
PORT1 DISAB:X|  I/O MAPPING:X|RUN TYPE1:
T&FBIU 1  2  3  4  5  6  7  8|I/O BD:01
DETBIU 9 10 11 12 13 14 15 16|COM BD:40
```

Note: The above screen will only display status messages which apply to the installed controller components. For example, if a particular controller is equipped with a TS-1 comm module, TS-2 status information (such as MMU and BIU status) will not be displayed.

I/O MODES STATUS DEFINITIONS:

MMU DISABLE.....X = MMU is disabled through keyboard programming, indicating the cabinet is not utilizing a TS-2 MMU.

MSA I/O MODE..... Indicates the I/O Mode (0-7)by activity of three I/O Mode select inputs on MSA.

PEER POLLING.....X = Indicates PEER-TO-PEER POLLING is active.

PORT 1 DISABLE...X = Indicates PORT 1 communications is disabled, through keyboard programming, indicating the cabinet is not utilizing TS-2 PORT 1 and is operating in the TS-1 mode.

I/O MAPPING.....X = Indicates Custom input and output configurations are enabled which.

RUN TYPE 1.....X = Indicates that the Type 2 Controller has been programmed to operate as a Type 1 controller. Thereby, Diabling inputs and outputs through MSA, MSB, and MSC since Type 1 controllers do not have these connectors. This feature does not aplly to Type 1 Controllers.

T&F BIU.....X = Indicates that a particular T&F (Terminals & Facilities) BIU (Bus Interface Unit) has been programmed to to be active, thereby communicating through Port 1 to the controller.

DET BIU.....X = Indicates that a particular Detector rack BIU (Bus Interface Unit) has been programmed to to be active, thereby communicating through Port 1 to the controller.

I/O BD..... Identifies the installed I/O Board, as follows:

- 01 = TS-2 Type 2
- 09 = LMD40
- 50 = TS-2 Type 1
- 78 = TCT1700
- FF = LMD8000

COM BD..... Identifies the installed COMM Board, as follows:

- 00 = TS-1
- 40 = TS-2
- 80 = Fiber Optic

PHASE INPUT STATUS DISPLAY

Selection 2 (I/O STATUS)....PHASE INPUTS

```
PH  1 2 3 4 5 6 7 8 |PH  1 2 3 4 5 6 7 8
IND r G r r r G r r |VOM           X
VEH M X X X M X X X |POM   X
PED   R   M   R     |HLD   X         X
```

PH.....Phase 1-8

IND..... Active indications, where:

- r = Red when other phases are being serviced
- R = Red Clearance (of that phase)
- Y = Yellow
- W = Walk
- D = Don't Walk
- G = Green
- N = This Phase Next

VEH..... Status of veh call where:

- X = Input active (LOW)*
- M = Call stored in memory, the controller is requested to serve the phase. Note that CNA and min recall (input) are considered constant calls stored in memory and would display a constant "M". Input triggered calls with "memory on" would display an "M" when not in the phase and the input is not active (see note following).
- R = Phase is programmed for recall; max recall, recall ext, etc (see note below).

* **Note**: An active input has the highest priority on the display. An "X" will replace "M" or "R" when the Veh input is active. **Also see** the "detectors" run screen.

PED.....Status of ped call where:

X = Input active (LOW)*

M = Ped Call stored in memory, the controller is requested to serve the ped. Note that CNA is considered a constant call stored in memory and would display an "M". CNA will cause an "M" for both the ped and vehicle.

R = Ped is programmed for Ped recall.

* **Note**: An active input has the highest priority on the display, i.e. an X will replace "M" or "R" when the Ped input is active.

VOM.....Vehicle Omit: "X" indicates input active.

POM.....Ped Omit: "X" indicates input active.

HLD.....HOLD: "X" indicates input active.

PHASE OUTPUTS DISPLAY

PG DWN..... OR Selection 3 (I/O STATUS).....PHASE OUTPUTS

```
PH  1 2 3 4 5 6 7 8 |PH  1 2 3 4 5 6 7 8
RED X   X X X   X X |DW  X X X X X X X X
YEL   X       X     |WLK
GRN                 |NXT     X       X
```

PH..... Phase 1-8

RED, YEL, GRN etc....."X" indicates the corresponding output is *called by the program* to be active (NXT = "this phase next" output).

NOTE: The indicators are driven by software, indicating the program has called for action. If there is a ***hardware failure***, however, the output may not actually respond.

PG DWN.....PHASE INDICATION/ON/CHECK and..... OVERLAP OUTPUTS

```
PH  1 2 3 4 5 6 7 8 |O/L  A B C D
IND R R G R R R G R |RED  X X X X
ON      X       S   |YEL
CHK   X       X     |GRN
```

PH.....Phase 1-8

IND..... Active indications, same as input status display.

On.....Phase on: "X" indicates output active

CHK.....Phase check: "X" indicates output active

O/L..... Overlap A, B, C, D

RED, YEL, GRN..... Overlap outputs; "X" indicates output active.

RING/UNIT INPUT STATUS DISPLAY

PG DWN OR Selection 4 (I/O STATUS)...RING/UNIT.....

```
FUNCT PH IND |MX2 FRC ST IMX RRM PDR ORC
RING1  2  G  | X
RING2  6  G  | X
INTVL R1: MIN   3  | INTVL R2: MIN 3
```

Shows Input status for per ring inputs.

PH.....Phase 1-8

IND..... Active indications, where:

R = Red
Y = Yellow
W = Walk
D = Don't Walk
G = Green

MX2..... MAX 2 input: "X" = input low in that ring.

FRC..... Force off input: "X" = input low in that ring.

ST..... Stop Time input: "X" = input low in that ring.

IMX..... Inhibit Max input: "X" = input low in that ring.

RRM..... Red Rest Mode input: "X" = input low in that ring.

PDR..... Ped recycle input: "X" = input low in that ring.

ORC..... Omit Red Clear input: "X" = input low in that ring.

INTVL R1/R2.....Indicates the active ring interval timing

MIN = Min Green (initial) timer
WLK = Walk timer
PCL = Ped clearance timer
MX1 or 2 = Max 1 or 2 timer
MP1-8 = Max Plan 1-8 timer in effect for phase
MF1-8 = Max Fail 1-8 timer in effect (det failure)
YEL = Yellow timer
RED = Red Clearance timer

PG DWN after Selection 5 (I/O STATUS)....PER UNIT..

INT ADV	MCE	EXT ST	CNA 1 2	WRM	MIN REC	TST ABC	FLO	CVM	FLT MON
							X	X	X

--PER UNIT STATUS--

X = Input/Output Active

SINT ADV..... Interval Advance (Input)
MCE.....Manual Control Enable (input)
EXT ST..... External Start (input)
CNA 1, 2..... Call to non-act 1 and 2 (inputs)
WRM.....Walk Rest Modifier (input)
MIN REC..... Minimum Recall (input)
TST A, B,C..Test Input A, B, C
FLO.....Flashing Logic Output (output, X = on/off)
CVM.....Controller voltage monitor (output, X = OK)
FLT MON.... TS-2 Fault Monitor (output, X = OK)

PRE-EMPT I/O STATUS DISPLAY

PREV MENU..Selection 5...**PRE-EMPT IN/OUTS..**

--PREEMPT INPUT/OUTPUT STATUS--

PE FUNC	-PRE-EMPT INPUTS- 1	2	3	4	5	6	-PRE-EMPT OUTS- 1	2	3	4	5	6
STAT	X						X					

X = Input Active

DETECTORS

Prior Menu...selection 6

Note that the following status screens apply to detector status at the *input level.* Phase level status of calls may also be viewed at the phase level from the phase inputs status display (prior menu....Phase Inputs).

DET INP	1	2	3	4	5	6	7	8
STATUS	1	2	3	4	5	6	7	8
DELAY	0	0	0	0	0	0	0	0
STR/DIS	0	0	0	0	0	0	0	0

PG DWN for detectors 9 - 64

DET INP	9	10	11	12	13	14	15	16
STATUS	X0	X0	X0	X0	X0	X0	X0	X0
DELAY	0	0	0	0	0	0	0	0
STR/DIS	0	0	0	0	0	0	0	0

This display is used to observe phase detector 1-24 input status, where:

DET INP = Detector inputs 1-64
STATUS = **First character** (alpha):
X = input active
M = Call stored in memory*
F = Detector has failed
Blank = No input active, no call in memory
Second character (numeric):
0-8 = phase input assigned to (0= none)

***Note** that in order to see memory on at the input level, it must be *programmed on at the input level.* If memory is on at the phase level only, memory on (M) will not appear on this screen (see phase inputs display...prior menu).

DELAY = Delay timer timing (times during red only, times down only when input *is active).*
STRETCH = Stretch timer timing (during green only, times down only after input *goes away*).PER UNIT STATUS DIS
DISCONNECT = Disconnect timer timing (during green only, times down only after input *goes away*).

QUEUE DETECTOR STATUS

This screen is active when ADAPTIVE SPLIT CONTROL is used and splits are select by the size of the waiting vehicle QUEUE .

--QUEUE DETECTOR STATUS--

PHASE	1	1	2	2	3	3	4	4
Q DET	0	0	0	0	0	0	0	0
Q DELAY	0	0	0	0	0	0	0	0

PG DWN... for PHASES 5 - 8

Q DET = Indicates which two queue detectors are assigned to a particular phase.
Q DELAY= The delay timer times down when the detector input is low (active).

VOLUME LOGGING RUN STATUS SCREEN

Page down from the QUEUE DETECTORS status screen, or…hit MAIN MENU-RUN MODE—RUN MODE DISPLAY —I/O STATUS—DETECTORS (MAIN MENU-1-1-6-6-PGDN *5 times*) to get….

```
# REC S AVAIL: T1:   0  T2:   0  TOT:  0
DET INP   1      2        3          4
  VOL      0      0        0          0
                    --PGDN TO CONTINUE--
```

PG DWN ETC. through detectors 5-64.

The top row of the display shows the number of records available for the T1 (telephone 1) and the T2 (telephone 2) buffers and the total. The volume counts are per the sample period, i.e. they zero out at the beginning of each new sample period. A volume log sample period must be programmed to produce counts.

TIME CLOCK CIRCUIT STATUS

The screens appear as shown below, are accessed through the I/O STATUS DISPLAYS menu or PG DWN from the Detector Volume Logs.

```
-TIME CLOCK CKT RUN MODE--(X=CIRCUIT ON)
   CKT    8   9  10  11  12  13   14  15
 FUNCT  FL  AX1 AX2 AX3 AX4 SYS  MX2 IM1
  STAT        X               X    X
```

X= CKT is on

PG DWN….

```
-TIME CLOCK CKT RUN MODE--(X=CIRCUIT ON)
   CKT   16  17  18  19  20  21   22  23
 FUNCT  IM2 CN1 CN2 MIN VC1 VC2  VC3 VC4
  STAT        X
```

X=CKT is on

Etc…Continue paging down through all circuits. Refer to CLOCK CIRCUIT DESCRIPTIONS in TIME CLOCK PROGRAMMING Section.

INPUTS

Prior Menu…selection 8…….

The input status screens display the current activity all physical inputs. Since inputs can be “AND”ed and/ “OR”d with other inputs and outputs, the activity of those associated inputs is also displayed. An asterisk (*) indicates activity. See Application Chapter for complete definitions. PAGE DOWN through several screens of the following list of inputs:

Function	Description
VD1-32	Vehicle detectors 1-32
PED1-8	Pedestrian detectors 1-8
HLD1-8	Phase hold 1-8
VOM1-8	Vehicle phase omit 1-8
POM1-8	Pedestrian phase omit 1-8
PRE1-6	Pre-empts 1-6
WRM	Walk rest modifier
MRCL	Min recall
SG/CS	Simultaneous gap-out inhibit/ Conditional service
WP10	Call to week program 10
ASQA-D	Alternate sequence A-D
MCE	Manual control enable
IADV	Interval advance
EXST	External start
TSTA-C	Test A, B, or C
DIM	Dimming function
LAMP	Indicator lamp control
MONA-C	Conflict monitor status bits A-C
MONF	Malfunction Management Unit flash
LCFL	Local flash
FLM1-2	Flash monitor 1 & 2
PLANA-D	Timing plan A-D
OFF1-3	Offset1-3
TBC	Call to clock
CTF	Call to free
SNCI	Sync inhibit
CSYS	Call to system
TSNC	Time clock sync
ITCI	Interconnect inhibit
AUTF	Automatic (remote) flash
CNA1-2	Call to non-actuated 1-2
FRC1-2	Force-off ring 1 & 2
IMX1-2	Inhibit MAX timing ring 1 & 2
MX21-2	MAX timing ring 1 & 2
ORC1-2	Omit red clearance ring 1 & 2
PCY1-2	Pedestrian re-cycle ring 1 & 2
RRM1-2	Red rest ring 1 & 2
STM1-2	Stop time ring 1 & 2
UDA	User defined 1-8
ADR0-7	Address bits 0-7
VD33-64	Vehicle det’s 33-64 (not used)

OUTPUTS

Prior Menu...selection 9.....

The output status screens display the current activity of all physical outputs. An asterick (*) indicates activity. See APPLICATIONS chapter for complete definitions. PAGE DOWN through several screens of the following list of outputs:

Function	Descriptions
Phase 1-8	Red/yellow/green drivers
Overlap	Red/yellow/green drivers
Ped 1-8	Don't walk/ped clear/walk outputs
Phase 1-8	Check/next/on outputs
PLNA-D	Timing plan A-D
OFF1-3	Offset 1-3
FLC	Call Flash
AUX1-4	Auxiliary time clock circuits
HOLD	Hold output
SYS	System out
SYSC	Call to system
PE1-6	Pre-empts 1-6
FL	Flash out
FLO	Flashing logic out
CSA-C1	Coded status bit A-C ring 1
CSA-C2	Coded status bit A-C ring 2
FFL	Fast flash status
FFLO	Fast flash logic
ADW1-8	Advanced warning 1-8
ADWA-D	Advanced warning A-D
SF1-24	Special function bit 1-24
CNT0-3	Display contrast
EL	Display light
CVMI	Controller voltage monitor
FMI	Fault monitor
DS1-16	Detector simulator outputs 1-16
PE ACK 1-6	Pre-empt acknowledge 1-6
CHAN 1-8 RYG	Channel 1-8 output designations

CODED STATUS BIT DISPLAY

PG DWN... or....Back to Run Mode Menu....Selection 7...CODED STATUS

```
     --CODED STATUS BIT DISPLAY--
 BIT  A B C |STATE |PH |IND|MODE|INTERVL
RING1 X     |MIN   | 4 | G |ACT |MIN   3
RING2 X     |MIN   | 8 | G |ACT |MIN   3
```

BIT A, B, C..... Coded Status Bits; "X" = bit active

PH.....Phase 1-8

IND..... W, G, D, Y, R (active indications)

MODE..... CNA or Acttuated

INTERVL..... Indicates the active interval ring timing:

- MIN = Min Green (initial) timer
- WLK = Walk timer
- PCL = Ped clearance timer
- MX1/2 = Max 1 or 2 timer
- MP1-8= Max plan 1-8 timer
- MF1-8= Max Fail 1-8 timer (detector has failed)
- YEL = Yellow timer
- RED = Red Clearance timer

STATE.....State Phase is in, varies depending on act or non act status of the phase as follows:

ACTUATED PHASE

DEC CODE	BIN CODE A	B	C	STATE	DESCRIPTION
0				MIN	Min Timing (MIN GRN, WLK, PCL)
1	X			EXT	Extension timing
2		X		MAX H	Max timing, hold applied*
3	X	X		GRN R	Green rest (max not timing)
4			X	YEL	Yellow timing
5	X		X	RED	Red Clearance timing
6		X	X	RED R	Red Rest
7	X	X	X		Pre-empt special interval

* Passage timer has timed out, max timer may also be timed out, but hold is applied

NON-ACTUATED PHASE

DEC CODE	BIN CODE A	B	C	STATE	DESCRIPTION
0				WLK	Walk Timing
1	X			WLK H	Walk timed out, hold applied
2		X		PCL	Ped Clearance timing
3	X	X		GRN R	Green rest
4			X	YEL	Yellow timing
5	X		X	RED	Red Clearance timing
6		X	X	RED R	Red Rest
7	X	X	X		Pre-empt special interval

PHASE SERVICE

PG DWN OR PRIOR MENU...Selection 8....PH SERVICE

```
      --PHASE SERVICE DISPLAY-- (PGDN)
PHASE    1   2   3   4   5   6   7   8
ON/OFF   ON  ON  ON  ON  ON  ON  ON  ON
RECALL  EXT CNA MAX PED FMX CNA DET PED
```

The display indicates the phases used and the mode of service, i.e the reason the phase is being service. Much of this information *could be* determined from the program menu, but the phase service display is simply a *more convenient* way of doing so without having to search through and evaluate several program menu screens.

The phase service display also indicates when a phase is in the CNA mode--which is a function of *both programming and input action.*

ON/OFF..... Indicates if the phase is used or not

RECALL..... Indicates the method of service, where:

- EXT = Extendible recall programmed
- MAX = Max recall programmed
- FMX = Fail Max Recall (a detector has failed)
- PED = Ped recall
- SFT = Soft recall
- CNA = Phase is programmed CNA & input is active
- DET = Phase is actuated, depends on detection
- MIN = Phase call due to External Min Recall

Notes:

1.Soft Recall provides a call similar to recall extendible--butonly if no other "real" calls (by detector actuation) exist. Typically used on main street in fully actuated (almost) application so that controller will rest in main street in the absence of any other real calls, but will not serve main if other calls exist and no "real" (detector actuated) call on main. To use soft recall, all phases must be actuated, including the soft recall phase (i.e. main street must have detection).

2. CNA, in its standard usage, is a function of programming and input action. Thus, CNA on the display indicates the phase is actually operating in the CNA mode.

3. Fail Max Recall (FMX) occurs when detector monitoring is used and the associated detector falls out of range. The Fail Max value is determined from the active max plan which has a second max setting per phase for this purpose. Max Plans must be used for this feature to operate.

Page down from phase service display...

SERVICE PLAN, MAX PLAN STATUS...

```
  --PHASE SERVICE DISPLAY CONTINUED--
FUNCTION: SERV PLAN| MAX PLAN |SEQUENCE
  STATUS:    1     |    1     |DUAL RING
SELECTOR:   CLK    |   CLK    | CS0 111
```

This display indicates the current Service Plan and Max Plan in effect and their mode of selection. The current sequence in effect as well as CSO are also indicated.

SELECTOR: CLK = selected by time clock circuit
C/S = selected by Cycle and split

SEQUENCE: Current sequence in effect

CSO: Current cycle, split, and offset in effect

COMMUNICATIONS STATUS DISPLAY

The communications status display provides detailed real time status of the communication port, the modem port (Port 3), HSSP (Port 1)and the RS-232 port (Port 2). The screens are accessed from the Run Mode Menu, selection 9.

Select **COMM STATUS** from the run mode menu....

First screen.....Last call in status

```
LAST CALL STAT:                    |13:52:05
RETRY 1: 4 |SCHED    |      A   B   C   V
RETRY 2: 4 |PHONE    |DEL    0   0   0   0
```

This screen is used when the LMD is used with a dial-up modem or direct RS-232 and directly reports to a central IBM or comapatible PC.

The display shows the status of the last attempted call-in, where:

RETRY TMR 1/2 = The retry timer for phone number 1 and 2 respectively. If a phone call is attempted, but cannot be completed, the retry timer will begin timing a 4 minute period before trying again.

SCHED = Schedule A, B, C, V (volume logs), or MOE's, (measures of effectiveness)

TIME = Time of day call was (is) attempted

STATUS = Status of the last call (or active call) from the controller's perspective.

Dialing initial....setting up communications

Dialing.....when dialing

Call Failure.....did not connect (error, busy)

Xfer failure..... An error in the handshaking

Xferring...Data being transmitted

Completed...Call has been completed

N/A: MDM....MDM system, no direct dial

DELAY 0 = no calls waiting to be called in

1-255 = call in delay timer in minutes

* = delay timer has timed out, schedule will be called in on next attempt.

PG DWN...System Comm Info

MDM-100 System Comm Info (if MDM-100 is selected for System Type in Comm Set-up)

```
Sys:        Sect:  1   SYSTEM C/S/O: TBC
HOL:        Int:   1
            Tmr:   0   ACTUAL C/S/O: Free
S/F: -------- -------- --------
```

Sys: X = Master is issuing sectional commands to the intersection.

HOL X = Master is issuing coordination commands.

Sect: 1-4 = Indicates which section the intersection is opperating under (issued by master)

Int: Intersection entered in COMM SET-UP

Tmr: 15 second timer, if comm is lost, intersection will revert to local time base control

SYSTEM C/S/O: The cycle/split/offset combination being issued by the master

ACTUAL CSO: The actual cycle/split/offset combination (or free) implemented at the intersection

S/F X = An active special function bit issued by the master. The "X" will be displayed above the lines indicating bits 1 - 24.

LM-100 System Comm Info (if LM-100 is selected for System Type in Comm Set-up)

```
Sys:        Sect:  1   SYSTEM C/S/O: TBC
 FL:        Int:   1
            Tmr:   0   ACTUAL C/S/O: Free
S/F: ----
```

PG DWN....Modem ports status

```
      Cnt  Data       Port: Modem  DCD:
Send:  22  1C22       Mode: SYS    CTS:X
Rcv:   11  3D44       Errs:  0     DTR:
LCR:       26E4       Stat: 02     RTS:X
```

PG DWN...RS-232A (page down for RS-232B if equipped) port status....

```
      Cnt  Data       Port: RS232A DCD:
Send: 191  0000       Mode: XFR    CTS:
Rcv:  196  1100       Errs:  0     DTR:X
LCR:       0009       Stat: 02     RTS:X
```

The display operates continuously during any of the following communications activities:

FUNCTION	PORT	MODE
Unit to unit data transfer	RS-232A	XFER
Direct PC up/download	RS-232A	XFER
Direct call-in to PC	RS-232A	XFER
Unit to serial printer	RS-232A	PRINT
LM/MIST Comm	Modem	LMSYS
MDM/MIST Comm	Modem	MDMSYS
LNME Upload	RS232B	MON

KEYBOARD FUNCTIONS

To reset all variables, press the **CLEAR** key.

To freeze variables, press and hold the **DECIMAL** key.

FUNCTION DEFINITIONS

Cnt: The number of bytes

Data: The hex value of the transmitted data

Send: data being sent over the medium

Rcv: data received over the medium

Note: When in the closed loop system mode, data is exchanged between the master and numerous local controllers. Activity shown on the display represents all activity on the common medium. Thus, only a portion of the total activity relates directly to this unit (see LCR).

LCR: Last Command received. This is the hex value of the last data received by this unit.

Port: Modem or RS-232

Mode: SYS for closed loop system normal communications, or XFER for data transfer, either thru the RS-2322, or, via the modem port when a remote upload/download thru the master takes place.

Errs: The number of detected errors since the last time the display was cleared.

Note: Do not be alarmed if occasional detected errors occur. A detected error is simply an indication that some portion of the transmitted data did not pass one of the error checking routines and was therefore not accepted by the receive unit. The same data would be re-transmitted within a short time period. Communications lines are not perfect and some errors are to be expected. However, errors accumulated at a rapid rate (say more than 5 an hour) are an indication that there may be problems with the communications system.

Stat: Status of communications. Many of the status codes are meaningful only to TCT personnel, however, listed below are some of the more common codes that might be encountered:

Mode	Code	Description
MDMSYS	07	Normal, OK
SYS	01	Mode error (Sys vs. Xfer)
SYS	02	Normal, OK
SYS	1f	Recv'd message out of sequence
SYS	2f	Illegal command
SYS	3f	CRC error
XFER	14	New packet has been recv'd (OK)
XFER	46	Loss of carrier during transmission
XFER	47	Abort
XFER	48	Terminated session (OK, complete)

MODEM CONTROL FUNCTIONS

The following control functions are indicated *as they are used* in the LMD.

DCD: Data carrier detect, X = On during any data transmission

CTS: Clear to Send, X = On during any data transmission

DTR: Data Terminal Ready, X = On, the X pulses briefly (and faintly because of the brevity) during SYS mode (closed loop system), On steady during any other data transmission when communicating

RTS: Request to send. X= On during any data transmission when communicating.

FAULT STATUS

Return to top run mode menu.....

```
        --BASIC STATUS MENU--
1.RUN MENUS     4.PRE-EMPT  7.MMU STATUS
2.FAULTS        5.MOE STATUS
3.CLOCK STATUS  6.SCHED LOGS
```

Selrction 2.....FAULT STATUS.....

```
        -- FAULT STATUS --
                |
        NO FAULTS DETECTED
                |
```

POSSIBLE FAULTS

Checksum Failure

Indicates if any checksum errors are present. A checksum error is an indication that 1 or more bits of program memory have changed improperly. The specific area in which the checksum error occurred will be indicated.

The CVM output goes Hi (false) and the intersection is placed in flash when checksum failure occurs.

If a checksum failure has occured, "CKSUM LATCH" will be displayed on the Run Mode Basic Status Screen, in the lower right corner.

NOTE: If a checksum failure has occurred:

1. Go to the program menu corresponding to the faulty checksum area.

2. Check all data fields in that area, re-program as necessary. If the data has been severely disturbed, go to the utilities menu and clear the area and re-program the entire area, or use one of the back-up plans.

3. After re-programming, the checksum will be cleared, however, the controller will not clear the CVM failure (output is still Hi) until a restart code is executed (utilities menu) or power down & up.

See Fault List on page 3-4 for a complete listing.

CLOCK CONDITION

Return to top run mode menu

CLOCK CONDITION.... Selection 3....Indicates when the time clock is normal or when it is updating events to the present time:

```
--TIME CLOCK STATUS--

TIME CLOCK IN NORMAL OPERATION--
```

It may also inform you that the clock events *need to be updated*, or that the clock *needs to be set.* if so, simply hit Prior Menu, which will take you to the clock menu. Proceed from there and select the appropriate menu.

PRE-EMPT STATUS

PRE-EMPT ACTIVE (during Power-up).....

If a pre-empt input is active during power-up, the following message will appear in the lower right corner of the display.....

```
PHASE/OL 1 2 3 4 5 6 7 8 A B C D | CYCLE
SPD      r G r r r G r r r r r r | W XYZ
MIN XY   WLK XY |MIN XY   WLK XY |PREMPT
MX1 XY   PSG XY |MX1 XY   PSG XY |ACTIVE
```

Followed by SEE HELP.....(Press HELP).....

```
Preempt during Start Up Flash. Preempt
input is active or was latched. Flash
will continue until input not active, or
until restart if input was latched.
```

Return to top run mode menu

PRE-EMPT STATUS....Selection 4....

Indicates when the LMD is entering, or is in pre-emption. When in pre-emption, it will display the pre-empt sequence step in effect, the timer, hold status, and pre-empt output status:

```
--PRE-EMPTION STATUS--    SEQUENCE  1
STEP |PH'S SPECIAL|TIMER |HOI |OUTPUTS
  1  |26          | 10   | ON | 1
--PG DN TO SEE PE INPUT STATUS--
```

STEP = The number of the pre-empt instruction step 1-15.

PH'S SPECIAL = The active phase(s), special interval, or code (such as 90, which is all red).

TIMER = The active pre-empt interval timer. When timing, the conditions specified by the instruction will be maintained. When timed out, the next step will begin, unless "HOI" is active, in which case the timer will hold at zero (same step).

HOI = Hold On Input. When on, the unit will remain in the current step until the input goes away. The timer will hold at zero.

OUTPUTS = Shows corresponding number of any active PE outputs. A flashing digit indicates the output is in the flash mode.

PG DWN.....Pre-empt input status:

```
 PE/(PRI)  1(1) 2(2) 3(6) 4(6) 5(6) 6(6)
ACTIVITY    X          M
DELAY TIME   0    0    0    0    0    0
MIN RESERV   0    0    0    0    0    0
```

The display shows the pre-empt input activity, priority assigned, plus the delay and min reservice timers. Note that omits may be applied the "last X" seconds of the delay timer (see pre-empt programming):

PE/(PRI) = The value inside parenthesis indicates the priority of the sequence (1= highest).

ACTIVITY = X indicates an active PE input. M indicates a call is stored in memory.

DELAY TIMER = Delay before pre-empt timer.

MIN RESERV = Min reservice timer (minutes). When used, this timer begins after service of the Pre-empt seuence and disallows that sequence again until it times out.

MOE STATUS

Return to top run mode menu.....SELECTION 5.....

A number of MOE status screens have been provided to view the accumulation of data as well as to aid in setting up MOE parameters. **NOTE:** MOE status screens may be observed even though clock ckt 141 is not on, i.e. the LMD does not have to be *logging* MOE's. However, a **sample period must** be programmed, and speed traps and computed speeds do **require set-up programming.**

From MAIN MENU, Select the RUN MODE submenu....

```
          --BASIC STATUS MENU--
1.RUN MENUS     4.PRE-EMPT  7.MMU STATUS
2.FAULTS        5.MOE STATUS
3.CLOCK STATUS  6.SCHED LOGS
```

SELECTION 5....MOE STATUS

```
          --MOE STATUS MENU--
1.SPEED TRAPS       3.GRN DATA/VOL
2.COMPUTED SPEED    4.MAX'S/FO'S/GAP'S
```

SPEED TRAPS

SELECTION 1....SPEED TRAPS....The following run status screen pertains to speed trap information (see page 3-51).

```
--SPEED TRAPS; UNITS= MPH--
 TRAP    A     B     C     D  |USE KEYS;
L SPD     0     0     0     0  |"." = FREEZE
A SPD     0     0     0     0  |CLR = RELEASE
```

Information on the screen relates to the *current period* as it is computed, where:

L SPD = The last speed trap event registered

A SPD = The average trap speed thus far in the period.

Note: the display can be *frozen* by hitting the decimal key, and *cleared* by the CLR key. The Average speed value will **automatically clear** at the end of the sample period.

COMPUTED SPEED

SELECTION 2....COMPUTED SPEED. The following run status screen pertains to computed speed information (see page 3-52 for programming).

```
COMPUTED SPEED; UNITS= MPH, OCC= SEC/100
DET INP  1   2   3   4   5   6   7   8
C SPEED  0   0   0   0   0   0   0   0
   OCC   0   0   0   0   0   0   0   0
```

PG DWN FOR DETECTORS 9-64

Information on the screen relates to the *current period* as it is computed, where:

C SPEED = The last computed speed value

OCC = The last occupancy in sec/100

Note: The occupancy values can be used to calibrate the detectors (see computed speed programming)

GREEN DATA/VOLUME

SELECTION 3....GRN DATA/VOL. The following run status screen pertains to green data and volume information.

```
  PHASE    1        2        3        4
AVE GRN    0        0        0        0
GRN UT%    0        0        0        0
   VOL     0        0        0        0
```

PG DWN for phases 4-8.

AVE GRN = The average of actual greens used thus far in the period.

GRN UT %= The average green % utilized thus far in the period (as a percentage of the green allocated).

VOL = The accumulated volume of all detectors assigned to the phase (EXT phase) thus far in the period.

NOTE: All Green/Vol data on the screen will **automatically clear** at the end of the sample period.

MAX'S/F.O.'S/GAPS

SELECTION 4....MAX'S/F.O.'S/GAPS. The following run status screen pertains to green data and volume information. No set-up programming is required.

```
 PHASE  1  2  3  4  5  6  7  8
 MAX'S  0  0  0  0  0  0  0  0
F.O.'S  0  0  0  0  0  0  0  0
 GAP'S  0  0  0  0  0  0  0  0
```

Shows current mix of MAX'S/F.O.'S/ GAPS thus far in the period.

SCHEDULE LOGS

Return to top run mode menu.....Selection 6.....

The Schedule Logs display provides the capability of viewing any stored function reports. In addition to being viewed on the front panel, these significant events can be called in directly (or through the MDM-100 System Master) to a central Office Monitor using LM System Software. For more information, see REPORTS later in this Chapter.

From MAIN MENU, Select the RUN MODE submenu....

```
        --BASIC STATUS MENU--
1.RUN MENUS     4.PRE-EMPT  7.MMU STATUS
2.FAULTS        5.MOE STATUS
3.CLOCK STATUS  6.SCHED LOGS
```

SELECTION 6....SCHEDULE LOGS

```
      --POINTER SELECT MENU--
  1.T1 POINTER
  2.T2 POINTER
```

Select the apprpriate telephone number to which the reports are to call (T1 or T2)...

```
      --SCHEDULE SELECT MENU--
   1.SCHEDULE A      3.SCHEDULE C
   2.SCHEDULE B      4.REQUEST
```

Slect the appropriate schedule (buffer) to which the function is stored and view any stored messages....

```
  DATE     TIME     MESSAGE (SCHEDULE A:T1)
01/07/92  07:39:03  POWER ON
02/09/92  22:46:45  UD INPUT 01 ON
04/05/92  15:22:02  DET 15 FAIL NO ACT
```

PG DWN for more messages.

MMU STATUS

Return to RUN MODE MENU.....

```
        --BASIC STATUS MENU--
1.RUN MENUS     4.PRE-EMPT  7.MMU STATUS
2.FAULTS        5.MOE STATUS
3.CLOCK STATUS  6.SCHED LOGS
```

Select .....7. MMU STAT(US).....

```
CH 1234567890123456|STATUS:CONFLICT
 R X XXX XXXXXXXXXX| RELAY:TRANSFERRED
 Y                 | RESET:  | RED ENAB:
 G  X    XX        | 24VMI:  | DATA RCV:
```

The above screen displays status information and indications from the MMU. This information is only valid if data is currently be received form the MMU, indicated by the DATA RCV : "X" (X is toggling).

MMU STATUS	NORMAL
	NORMAL/VMI (with 24 Volt inhibit)
	CVM FAILURE
	+ 24-I VDC FAILURE
	+ 24-II VDC FAILURE
	CONFLICT
	RED FAIL
	MMU DIAGNOSTIC FAILURE
	MIN CLEARANCE FAILURE
	NEMA + FAULT (any NEMA plus feature failure
	PORT 1 Fault
RELAY	NORMAL (no failures)
	TRANSFERRED (failures)
RESET	X = ON
RED ENABLE	X = ON
24 VMI	X = ON (24 volt monitor inhibit is active)

Page Down.....

```
--MMU PROGRAMMING CARD STATUS--
MIN YEL DISABLE  |MIN |CVM |24VM|
1234567890123456 |FLSH|LTCH|LTCH|
X                |  7 |    |    -PGDN-
```

The above screen displays programming card information. This information is only valid if data is currently be received form the MMU, indicated by the DATA RCV : "X" (X is toggling). The following features are activared by the presence of jumpers on the MMU programming card:

Any channels with Minimum yellow time disabled.

Minimum flash period

If CVM failure is a latched fault

If 24 VDC failure is a latched fault

Page Down.....

```
CH1 -------5-6-------------------------
CH2  ------5-6-------------------------
CH3    --------7-8---------------------
CH4      ------7-8---------------------
```

Page Down through channel 16

The above screen represents MMU programming card information, which is determined by programming card jumpers. For example a "5" in the channel 1 (CH1) row would indicate a 1-5 jumper on the card. This information is only valid if data is currently be received form the MMU, indicated by the DATA RCV : "X" (X is toggling).

ERROR CODES

Under certain conditions the LMD will display various error codes. In many cases these are codes which have been incorporated for use by the developer and are not of value to the end user. What follows is a brief discussion on the various error codes and conditions.

Comm Status Screen…'Stat' Field

The meaning of this field varies, depending on the Port's Mode. In most cases it displays the content of the byte in the port's buffer structure, which, because of its dynamic nature, is of little value to the end user. When port mode is MATS, MIST, or MDM100, and the port error count ('Errs' field) is non-zero, the field is overwritten and error information is displayed. In these cases, the 'Stat' field will display one of the following error codes:

1f – Invalid Message Structure Received
2f – Unrecognized Command Received
3f – CRC Error in Received Message
4f – No Reply from LNME During Monitor Upload

When 'CLEAR' is pressed, this screen is cleared. Since this also clears the 'Errs' count field, it will also cause the 'Stat' field to revert to its default mode (takes it out of error code mode) until the error count again becomes non-zero.

CPU Failure Screen

This screen appears when the processor suffers a catastrophic failure. Because of the nature of the failure only limited information is available, however the CPU does provide its best estimate of the possible error. None of these faults can occur under normal operation, so the most that can usually be inferred is that the problem is with one of the basic operating components; the CPU itself, the memory (RAM or PROM), or the Vcc supply. The possible error codes are as follows:

604 – Non-Maskable Interrupt Occurred
648 – Stack Overflow
64c – Memory Access Violation
654 – Privileged Instruction Violation

SECTION IV

PROGRAM/READ MODE

The program mode is used to program or read operational data. To access the program/read mode, select the "PROGRAM/READ MODE" option from the main menu and proceed through the menu screens until the desired data screen appears. When the desired data screen appears:

1. An arrow will point to the selected data field.

2. Use the arrow keys to move from one field to another.

3. Use "PGUP", "PGDN" to move from one screen to another.

4. Press the appropriate digits to key in a value. The cursor appears and flashes after keying in data until the data is loaded.

5. Press "ENTER" or *move the arrow* with arrow keys to load the data (moving the arrow in most cases has the same effect as "ENTER"). The cursor disappears as the data is accepted.

6. If the curser is still flashing, the new data has not been entered yet. Be careful to hit the arrow key or "ENTER" that last time on the last entry before paging to a different screen.

Data Entry Notes:

a. Some data entries will be numeric values such as "8" seconds minimum green, etc.

b. Some entries are ON/OFF, such as memory ON/OFF. The ON/OFF keys correspond to digits 1 (OFF) and 2 (ON).

c, Some data entries will be specified choices such as choice "1" is dwell mode offset seeking and "2" is shortway, etc. In such cases, the choices will be defined on the screen.

7. To repeat the same value in consecutive fields, load the initial value* to be repeated, then hold the ENTER key depressed while moving to new fields with arrow keys. The same value (as determined by the the initial value or last data keyed and loaded using the "ENTER" key) will be loaded into each new field. You may skip fields by releasing the enter key, then re-applying it on the next field to be repeated.

*The repeat value must be keyed and loaded, you cannot simply access a screen and start repeating existing values.

8. A 4 digit security access code may be required to enter or change data. If required, follow the security code menu and load the security code when prompted. The screen will inform you if your selection is accepted or not, or if not required, already loaded, etc.

BASIC PROGRAM PROCEDURE TO PROGRAM THE LMD CONTROLLER FROM SCRATCH

Note: We strongly recommend that when programming a controller from scratch, you do so in the shop, then transfer the programmed unit to the field.

1. Go to the Utilities menu, select the clear option and clear controller, coordination, and clock data (3 separate steps).

2. Go to the the PROGRAM/READ menu and, systematically proceed through each menu and load the desired data. Return to the screens when done to verify your entries.

3. If you have changed controller sequence, you must keyboard restart (utilities menu) or power down & up.

TO PROGRAM THE LMD CONTROLLER FROM BACK-UP PLANS ON PROM

Note: We strongly recommend that when programming major segments of a controller, you do so in the shop, then transfer the programmed unit to the field.

1. Go to the Utilities menu, select the back-up option and copy the controller, coordination, and clock data as desired. Note that under the controller or coordination options, you will be given choices of the number of phases. The 2, 3, and 4 phase options are single ring; the 5, 6, and 8 phase options are dual ring. Phase 2 in single ring, and phases 2 and 6 in dual ring applications are the coordinated phases (except for the 2 phase plan in which phase 1 is the coordinated phase).

2. If necessary, go to the the PROGRAM/READ menu and, proceed through each menu and edit the desired data from the back-up plans. Return to the screens when done to verify your entries.

3. When using back-up plans, you must keyboard restart (utilities menu) or power down & up.

TO SET THE TIME, DATE, YEAR

1. Go to the PROGRAM/READ menu, then select the Time clock menu

2. From the Time clock menu, select the Time Set menu.

3. Select the Time/Date menu.

Key in the time of day in 6 digits. Load the time slightly ahead of the real time and then hit enter at the precise moment.

Enter the year and date. The Year must be entered prior to the date. (The day of the week , among other things, is automatically calculated, and is a function of the date and year).

4. After loading the new time, you may wish to manually update the clock events to the current time you have just loaded. This will occur automatically ten minutes after the last keystroke, but you may wish to do it right away.

To update the clock, return to the prior menu and select "Update". The LMD will update the clock events and will indicate that it is updating. This process make take several minutes, however, so you may go about any programming or viewing other screens during the process. The "clock condition" screen from the Run Mode menu can also be selected to determine update completion.

Note that the update screen will prompt you to load the time and date if it determines that they are not correctly loaded.

PROGRAM DATA ENTRY SCREENS

To enter the program/read mode, return to the main menu...depress the "MAIN MENU" key.....

```
          --MAIN MENU--
1.RUN MODE            3. UTILITIES
2.PROGRAM/READ MODE   4.I/O CONFIGURE
      --USE HELP KEY FOR HELP--
```

To enter the PROGRAM/READ mode, enter selection 2.....PROGRAM/READ MODE

```
          --PROGRAM/READ MODE--
1. SECURITY CODE  4.TIME CLOCK   7.REPORTS
2. CONTROLLER     5.PRE-EMPTION
3. COORDINATION   6.COMM SET-UP
```

SECURITY CODE.

To enter the security code.....Selection 1...SECURITY CODE....

If a security code *is required*, the screen will prompt....

ENTER 4 DIGIT SECURITY CODE

If a security code is required *and a 4 digit code is loaded, but not accepted*.....i.e not the correct code,the screen will display;

SECURITY CODE NOT ACCEPTED

--HIT PRIOR MENU TO RET TO PROG MENU--

If a security code is *required, loaded, and accepted* ....the screen will display;

SECURITY CODE ACCEPTED:

1. RETURN TO PROGRAM MENU
2. LOAD NEW SECURITY CODE

--WHICH WILL BE REQUIRED IN FUTURE--

If *no* security code is required....the screen will display;

NO SECURITY CODE REQUIRED:

1. RETURN TO PROGRAM MENU
2. ENTER NEW SECURITY CODE

--WHICH WILL BE REQUIRED IN FUTURE

If the security code has *already been loaded*....the screen will display;

SECURITY CODE ALREADY LOADED

1. RETURN TO PROGRAM MENU
2. ENTER NEW SECURITY CODE

--WHICH WILL BE REQUIRED IN FUTURE

Note that to obtain the ability to load a new security code, you must load the old code, or it must have been already loaded (or there is no security code required). In other words, when required, you must know the old security code to load a new one. Load the code "1000" to inhibit the security code.

If the Security Code *was accepted or not required or already loaded* and selection 2 was chosen....the screen would prompt

LOAD NEW 4 DIGIT SECURITY CODE

--HIT PRIOR MENU OR MAIN MENU TO RETURN-

A new 4 digit security code can now be loaded.

Note: Be sure that you remember your security code. We don't make it easy to defeat the security code because that would defeat its intended purpose. However, should you forget your code, contact your nearest distributor or TCT, for instructions.

CONTROLLER PROGRAMMING

Return to PROGRAM/READ....

```
          --PROGRAM/READ MODE--
1. SECURITY CODE 4.TIME CLOCK  7.REPORTS
2. CONTROLLER    5.PRE-EMPTION
3. COORDINATION  6.COMM SET-UP
```

CONTROLLER...Selection 2.....

```
   --CONTROLLER PROGRAM/READ MODE--
1.MEMORY/RECALL/CNA 4.INITIALIZE/FLASH
2.PHASE TIMING      5.OVERLAPS
3.PHASING/SEQUENCE  6.DETECTORS/OPTIONS
```

MEMORY/RECALL/CNA

MEMORY/RECALL/CNA....Selection 1....

PH/INT	1	2	3	4	5	6	7	8
MEMORY	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
EXT REC	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
MAX REC	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

ON = function on, OFF = function off. **NOTE**: memory can also be applied per detector input 1-24, see Detectors/Options.

PG DWN

PH/INT	1	2	3	4	5	6	7	8
PED REC	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
CNA I	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
CNA II	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

PG DWN

PH/INT	1	2	3	4	5	6	7	8
FL WALK	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
SOF REC	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
WLK RST	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Note: Soft recall (vs. hard) applies recall ext. when no other "real" calls exist.

PG DWN

PH/INT	1	2	3	4	5	6	7	8
C. PED	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
FWTPCL	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Specify On or Off for each parameter. See Section I for other function definitions.

PHASE TIMING

PRIOR MENU.....Return to PROGRAM/READ Menu....

```
   --CONTROLLER PROGRAM/READ MODE--
1.MEMORY/RECALL/CNA 4.INITIALIZE/FLASH
2.PHASE TIMING      5.OVERLAPS
3.PHASING/SEQUENCE  6.DETECTORS/OPTIONS
```

Selection 2...PHASE TIMING...Load 0 to 127 or 0.0 to 9.9 (except MAX times which are 0-255 seconds)

PH/INT	1	2	3	4	5	6	7	8
MGR	7	15	10	10	7	15	7	10
PSG	3	4	3	3.5	3	4	3	3.5
YEL	4.5	4.5	4.5	4.5	4.5	4.5	4.5	4.5

PG DWN....

PH/INT	1	2	3	4	5	6	7	8
RED	0	2.2	0	2.2	0	2.2	0	2.2
MX1	20	25	15	25	20	25	20	25
MX2	50	25	15	25	15	25	15	25

PG DWN....

PH/INT	1	2	3	4	5	6	7	8
WLK	0	0	0	0	0	0	0	0
PCL	0	0	0	0	0	0	0	0
S/A	0	0	0	0	0	0	0	0

Load timing as required for each parameter. You may use decimal values from 0-9.9, or whole numbers from 0-127 (except MAX times which are 0-255 seconds)

PG DWN....

```
PH/INT   1   2   3   4   5   6   7   8
TBR      0   0   0   0   0   0   0   0
TTR      0   0   0   0   0   0   0   0
MIN GAP  0   0   0   0   0   0   0   0
```

PG DWN....

```
PH/INT   1   2   3   4   5   6   7   8
MAX VI   0   0   0   0   0   0   0   0
MAX EXT  0   0   0   0   0   0   0   0
AUTO MX  0   0   0   0   0   0   0   0
```

S/A = Seconds per Actuation
TBR = Time Before Reduction
TTR = Time to Reduce
MAX VI = Max Variable Initial

```
PH/INT   1   2   3   4   5   6   7   8
AMR      0   0   0   0   0   0   0   0

          --END OF SELECTION--
```

AMR = Added Max Red

PHASING/SEQUENCE

Return to Controller Program/Read Menu...

```
   --CONTROLLER PROGRAM/READ MODE--
1.MEMORY/RECALL/CNA 4.INITIALIZE/FLASH
2.PHASE TIMING      5.OVERLAPS
3.PHASING/SEQUENCE  6.DETECTORS/OPTIONS
```

Selection 3...PHASING/SEQUENCE.....

```
          --PHASES USED--
PHASE    1   2   3   4   5   6   7   8
ON/OFF   ON  ON  ON  ON  ON  ON  ON  ON
   --PGDN TO SET SEQUENCE SELECTION--
```

ON = Phase used
OFF = Phase not used (not serviced)

PG DWN....

```
     THE PHASING/SEQUENCE IS 2<
1.SEQUENTIAL          3-7.SPEC SEQUENCES
2.NEMA DUAL RING        8.LEAD/LAG
--PGDN FOR LEAD/LAG, PRIOR MENU IF NOT--
```

See Section II for descriptions of special sequences. If selection 8, LEAD LAG, then PG DWN.....

```
          --LEAD LAG--    | 1.NO REVERSAL
PAIRS   1&2 3&4 5&6 7&8   | 2.ALWAYS REV
CODE     1   1   1   1    | 3.REV BY C/S/O
   --PGDN TO CONT--       |   OR CLK/INPUT
```

1 = Normal NEMA operation (odd phase leads)
2 = Odd phase always lags
3 = Lead/lag operation determined by coordination or time clock (ckt's 88-91) or MSD inputs.

LEAD LAG BARRIERS ON = barrier between every pair.

INITIALIZE/FLASH

Return to controller Program /Read mode (PRIOR MENU).

```
   --CONTROLLER PROGRAM/READ MODE--
1.MEMORY/RECALL/CNA 4.INITIALIZE/FLASH
2.PHASE TIMING      5.OVERLAPS
3.PHASING/SEQUENCE  6.DETECTORS/OPTIONS
```

Selection 4...INITIALIZE/FLASH.....

```
      INIT |ENTR FL |EXIT FL |INTVL1=RED
R1 PH  2   |   4    |   2    |      2=YEL
R2 PH  6   |   8    |   6    |      3=GRN
INTVL  3   |   1    |   3    |  - PGDN -
```

Specify phases and interval for which the controller will:

a. Initialize

b. Enter Flash (the phases/interval served before flash)

c. Exit Flash

Note that the interval for flash entry is pre-loaded and is always 1 = RED, flash must be entered from Red.

Power-up and Restart timings

PG DWN..

```
    --POWER UP/RESTART TIMINGS--
 0  | MINIMUM FLASH
 0  | FIRST ALL RED AFTER POWER-UP
       --END OF SECTION--
```

Minimum flash is the guaranteed flash period after power interrupt or keyboard restart. **First all red** timing is used *once* after power-up or exit from remote flash (typically used when initializing in yellow or all red).

OVERLAPS

Return to controller Program/Read mode (PRIOR MENU.....

```
   --CONTROLLER PROGRAM/READ MODE--
1.MEMORY/RECALL/CNA 4.INITIALIZE/FLASH
2.PHASE TIMING      5.OVERLAPS
3.PHASING/SEQUENCE  6.DETECTORS/OPTIONS
```

OVERLAPS

Selection 5...OVERLAPS....(see overlap card option)

```
         --OVERLAP OPTIONS--
1.SET OVERLAPS      4.FAST FLASH RATE
2.DELAY OVERLAPS    5.OVERLAP CARD
3.O/L INHIBITS      6.PHASES AS OVERLAPS
```

Set Overlaps...selection 1

```
PHASE    1 2 3 4 5 6 7 8  | 0=NOT O/L
O/L A    0 0 0 0 0 0 0 0  | 1=O/L PH
O/L B    0 0 0 0 0 0 0 0  | 2=FAST FL
  --PGDN TO CONTINUE--    | 3=NOT PED
```

PG DWN for overlaps C & D.

Specify the overlap phases by entering a "1" corresponding to the overlap parent phases. Select 2 for Canadian fast flash. Select 3 for "not ped" (see definition below). The Fast Flash rate selection determines the rate of fast flash; selections include 60, 120, 150, and 180 FPM.

Overlap Delays

Prior Menu...Selection 2

```
    DEL YEL RED |CPH-OL |AW|ADD|DELAY IS
OLA   0 4.0 2.0 |  0/00 |0 |   |FROM PAR-
OLB   0 4.0 2.0 |  0/00 |0 |   |ENT PH Y
    --PG DN TO CONTINUE--     | TO O/L Y
```

PG DWN ....O/L's C and D. **NOTE:** CPH-OL, AW and ADD relate to advance warning (leave these 0 for delay only).

Overlap Inhibits

```
SEE HELP |PH/OL 1 2 3 4 5 6 7 8 A B C D
O/L A GRN|      0 0 0 0 0 0 0 0 0 0 0 0
O/L A YEL|      0 0 0 0 0 0 0 0 0 0 0 0
O/L A RED|      0 0 0 0 0 0 0 0 0 0 0 0
```

PG DWN for O/L's B, C, D. Inhibit codes are as follows;

0 = No Inhibit
1 = Inhibit during Green of indicated phase/overlap
2 = Inhibit during Yellow of indicated phase/overlap
3 = Inhibit during Red of indicated phase/overlap
4 = Inhibit during Grn + Yel of indicated phase/overlap
5 = Inhibit during Yel + Red Clr of indicated ph/overlap
6 = Inhibit during G + Y + Red Clr of indicated ph/OL
7 = Inhibit during WLK and PCL of indicated phase

FAST FLASH RATE (OVERLAPS)

This entry determines the Fast Flash rate of any overlaps set up to flash (selection # 4 in OVERLAP OPTIONS). The feature is generally used in Canada.

B.C. ADVANCE WARNING LOGIC

AW operation is provided by phases as overlaps and standard overlaps, where:

CPH-OL = Conditional phases/overlaps; 1-8 = phases 1-8, 9-12 = O/L A-D (9= O/L A etc.)

AW = ADVANCE WARNING ENABLE, 0= OFF, 1= ON

ADD = Advance Warning De-activation delay: 0-99 secs (time after green that AWL output de-activates).

AW Operation

1. Overlaps or phases as overlaps with delays are used to provide the feature. The advance warning *is the overlap delay period*. Enabled if AW= 1. For example, if phase 2 is desired to have advance warning, phase 2 driver would be set up as a phase 2 overlap with delay.

2. When AW= 1, MSD Clock ckt's are AW ckt's; Ph1 = Ckt 1, Ph 2 = Ckt 2...O/L A = Ckt 9, etc.

3. If AW= 1, for each overlap/phase as overlap, when the overlap delay period begins, the corresponding ckt is activated. (see conditional phase/overlap below). The Ckt stays on thru the timer, yellow, and red.

4. The CKT de-activates when it returns to green, after the ADD timer times out. ADD timer starts with green. If ADD = 0 the output de-activates immediately with the activation of green. ADD is used to compensate for queues.

5. CPH-OL = conditional phase-overlaps delay. Up to two per phase or overlap. If there are conditional PH/OL's specified, and if a conditional PHASES/OL's timer is timing* but is greater than the subject delay timer, then, the subject delay timer will not begin timing. The timer will thus "wait" (ckt remains off) until the active conditional phase delay timer has timed down to equal the subject phase time value. This allows two concurrent phases (or overlaps) to have different advance periods, yet *terminate* together.

* **Note:** The delay timer only waits if the conditional phase or O/L delay timer is timing or has been enabled to time, i.e. it is going to terminate. A delay timer may be *enabled* to time but *not actually timing* if that movement has another contingent PH-OL and is waiting as well. This allows *cascading* of advance warnings. The timer does not wait if the contingent phase is not going to terminate.

Overlap Card Option

LMD "N" version controllers are set up to use the NEMA overlap card (jumper on JP1, I/O board, about 1.5 inches above the RS232). Note that all overlap features, except the set overlap programming, are still available. Thus, it is possible to program overlap delays, fast flash, or overlap inhibits, while O/L programming is determined by the card.

Selection 5.....Overlap Card

```
      --OVERLAP CARD ENABLED--
O/L A      O/L B      O/L C      O/L D
PHASES     PHASES     PHASES     PHASES
```

The screen shown indicates that the card is enabled and is inserted, where O/L A is a 1+ 2 overlap and B is 1+ 3.
Note: When not set up for overlap card operation, the display will indicate **"OVERLAP CARD DISABLED".**

PHASES AS OVERLAPS

Prior Menu.....Selection 6....Phases as overlaps

```
OL/P 1 2 3 4 5 6 7 8|DEL |CPH-OL|AW|ADD
PH 1 0 0 0 0 0 0 0 0| 0  | 0/00 |0 | 0
PH 2 0 0 0 0 0 0 0 0| 0  | 0/00 |0 | 0
(0=NO O/L 1=OL PH)   .0= FAST FLASH
```

PG DWN ETC.....Through the remaining phases. The **delay time** represents the delay from parent phase yellow to O/L yellow. The overlap yellow and red used with the delay mode are the *normal* phase driver yellow and red.
Note 1: Delay = .0 = fast flash the green output.
Note 2: CPH-OL, AW, ADD used for advance warning only.

DETECTORS/OPTIONS

Return to Controller Program/Read menu (PRIOR MENU)

DETECTORS/OPTIONS.... Selection 6....

```
            --OPTIONS--
1. LCP/SGO MODE/DIM     4. 5 SECTION HEAD
2. R-REV/PED OPT/IY&R   5. SERV/MAX PLANS
3. DUAL ENT/COND SERV   6. DETECTORS
```

LCP/SGO MODE/DIM

Last car passage, simultaneous gap out mode..... selection 1

```
 --ON REDUCED GAP-OUT THE UNIT WILL 1<
 1.RECALL PHASE      3.NOT RECALL, NOT
 2.LAST CAR PASSAGE    LAST CAR PASSAGE
        --PGDN TO CONTINUE--
```

This function determines how the controller treats gap outs at reduced gap (with volume density gap reduction in effect). **Recall the phase** indicates that the phase will be recalled if gap out occurs at reduced level. **Last car passage** means that, once the controller decides to gap out at the reduced level, it will time additional green such that the last vehicle gets benefit of one full passage--but no further extensions are allowed. **No recall, no LCP** indicates that reduced level gap outs are not treated specially.

SIMULTANEOUS GAP OUT INHIBIT

PG DWN From previous screen....

```
-SIMULTANEOUS GAP OUT-| 0= PSG CAN RESET
PHASE 1 2 3 4 5 6 7 8 | 1= NO PSG RESET
CODE  0 0 0 0 0 0 0 0 | 2= INPUT DECIDES
          --END OF SECTION--
```

When programmed "1", a phase cannot reset its passage timer once it has gap'd out (and rests). Thus, once a phase gaps out–it will stay gap'd out. This affects dual ring operation when two barrier phases are about to cross the barrier and one is still extending while one rests.

Allowing the passage timer to reset (code 0) allows the resting phase's passage timer to begin timing again--even if the other phase is just about ready to gap out. In this case, both phases must *simultaneously gap out* in order for gap out to occur. Simultaneous gap out inhibit (code 1) generally results in "snappier" operation. Code 2 allows the decision to be made by DC input (0VDC = Passage timer cannot be reset).

DIMMING (PG DWN from previous screen....)

```
PH/OL 1 2 3 4 5 6 7 8 A B C D |0= NO DIM
  RED 0 0 0 0 0 0 0 0 0 0 0 0 |1= DIM +
  YEL 0 0 0 0 0 0 0 0 0 0 0 0 |2= DIM -
  GRN 0 0 0 0 0 0 0 0 0 0 0 0 | --PGDN--
```

PG DWN....

```
PHASE 1 2 3 4 5 6 7 8 A B C D |0= NO DIM
  WLK 0 0 0 0 0 0 0 0 0 0 0 0 |1= DIM +
   DW 0 0 0 0 0 0 0 0 0 0 0 0 |2= DIM -
  PCL 0 0 0 0 0 0 0 0 0 0 0 0 | --PGDN--
```

LMD phase and overlap driver outputs can be programmed for nighttime dimming to save energy and avoid glare. Each indication can be programmed to dim positive half wave, negative half wave, or not at all. The following general notes pertain to dimming:

-Dim activated by; TEST B, DC input, or CLK CKT (to use test B, see test B mode below).

-Care should be taken to insure that dimming **only occurs at night.**

-Care should be taken to **balance loads** between positive and negative half-waves, Consider indications likely to be on at the same time (e.g. main green vs. side red).

-**Only dim incandescent loads**. Never dim transformer driven loads such as NEON, HALOGEN, FIBER OPTIC, etc. These are most likely to occur on peds, so dim peds only when sure they will always be incandescent.

-**Do not dim 3M optically programmed heads** (they have their own dim capability).

RED REVERT/PED OPTIONS/ IY&R/ TEST B

PG DWN from previous or PRIOR MENU...Selection 2..

```
RED    |PED |FDW THRU|AUTO|% CKT 148|TEST
REVERT|ENH |  YELLOW |PCL |INC's Y&R| B
  0<+2|OFF |   OFF   |    |    0%   | 0
 SECS.| (TEST B: 0=DIM, 1=FREE, 2=F/DEL)
```

Red revert is the All Red period following yellow when a phase returns on itself (G-Y-R-G of same phase).

Ped enhancement is a special ped mode which applies to the Walk timing of CNA I programmed phases. For these phases, the walk timer uses **MAX timing** when **not** in CNA mode and uses the normal walk when CNA I input **is** applied. The Ped clearance times normally in either case. **Note;** Walk Rest Modifier **must be applied** for Ped enhancement to function.

Flashing Don't Walk thru Yellow, when enabled, will flash the Don't Walk indication thru yellow. It will go solid at the end of yellow (instead of at the end of green).

Automatic Pedestrian Clearance, when enabled, will protect the ped clearance time when the interval advance input is activated by a police door remote control switch (manual control enable active). Prevents skipping or short-timing ped clearance during manual control.

Increase Yellow & Red is a special function that allows all yellow and red intervals to be increased by up to 100 per cent.

Test B programming defines the the test B input function; 0= Enable Dimming, 1= Call to Free operation (disable internal coordination--often used with external comm units). 2= Call to Free also, **but with a 180 second delay** from the initial activation to the return to internal coordination. This prevents the LMD from attempting to return to internal coord after only a brief loss of comm at the RCU.

PEDESTRIAN OVERLAPS

```
O/L PED  1 2 3 4 5 6 7 8 | PED OVERLAPS
PH1 PED  0 0 0 0 0 0 0 0 | 0=NO PED O/L
PH2 PED  0 0 0 0 0 0 0 0 | 1=OVERLAP
   --PGDN TO CONTINUE--
```

PG DWN ETC.....Through the remaining peds. The default settings provide standard NEMA ped operation (all zeros).

Important Note: When an overlapping walk indication is about to overlap into the next phase, the ped timing **may be skipped if not needed** for any other peds that might be clearing at that time (i.e. the phase will terminate normally). The LMD will determine this from the overlapping

peds programming and active ped call status. Because the decision is derived from the overlapping peds programming, you must program any standard peds as overlaps if the standard ped phase is also an overlap parent phase. E.g. say in a 3 phase unit , there is a ph 1 ped, a ph 2 ped and a 1+ 2 ped. Set ph 1 and 2 ped drivers to overlap themselves and ph 3 ped driver as 1+ 2.

DUAL ENTRY

```
            --DUAL ENTRY--
PHASE        1  2  3  4  5  6  7  8
DUAL ENT PH  6  6  8  8  2  2  4  4
          --PGDN TO CONTINUE--
```

The Dual Entry phase is the phase called when the object phase (upper row) is called but there is no call in the opposite ring from that phase (DE phase is always in the opposite ring). **For the dual entry mode**....PG DWN....

```
 THE DUAL ENTRY MODE IS  1<
1.OFF  3. CALLED BY CNA    5.CALLED BY
2.ON   4. CALLED BY SYSTEM   T/C
      --PGDN TO CONTINUE----
```

1 = OFF–no dual entry
2 = ON–dual entry always on
3 = Dual entry in effect when CNA I or II inputs Lo.
4 = Dual entry called when LMD is in system
5 = Dual entry by clock CKT 57.

CONDITIONAL SERVICE/RESERVICE....PG DWN.....

```
   --CONDITIONAL SERVICE/RESERVICE--
PHASE  1  3  5  7 |0=BOTH OFF 3=IF NO SY
 MODE  0  0  0  0 |1=CS ON    4=BOTH ON
CSMAX  0  0  0  0 |2=CS/CL-IN 5=RS/CL-IN
```

Conditional service allows re-service (in the same cycle) of an odd phase (say phase 1) after the thru service when the opposite ring thru (say phase 6) continues to extend while the same ring thru (say phase 2) gap's out. The service is conditioned by the conditional service max time (C.S.MAX), such that there must be enough time in the still extending phase's (6) max timer to clear the gap'd out phase (2) with enough time to serve the conditional service max time of the re-serviced phase (1). The conditional service max timer becomes the max timer of the conditionally serviced phase (see Conditional Service, Section II).

Conditional Reservice allows return to the thru phase after the conditionally serviced left turn, otherwise stay in left turn then clear to serve cross street phases. Max times apply.

The codes for Conditional Service/Reservice are as follows:

0 = No Conditional Service or Reservice
1 = Full time Conditional Service only
2 = Conditional Service activated by clock circuit # 52
3 = Allow Conditional Service/Reserv when not in System
4 = Full time Conditional Service and Reservice
5 = Conditional Service and Reservice activated by clock circuit # 52

5 SECTION HEAD...PG DWN...

```
--5 SECTION HEAD RESTRICTIONS (ON/OFF)--
2 OMIT 5  4 OMIT 7  6 OMIT 1  8 OMIT 3
  OFF       OFF       OFF       OFF
        --PGDN TO CONTINUE--
```

These restrictions prohibit returning to left turn movements directly from the compatible thru movement without first servicing a side phase. Used with 5 section head protected/permissive left turns.

PG DWN....

```
  --5 SECTION HEAD YELLOW BLANKING--
PH  1   3   5   7  | ON = BLANK YELLOW
  OFF OFF OFF OFF  | IF CLEARS WITH THRU
        --END OF SECTION--
```

Applicable to dual ring control, prohibits the left turn yellow from coming on when the left turn clears simultaneously with the compatible thru movement (such as 1 and 6).

SERVICE/MAX PLANS

Service and Max Plans provide 8 additional sets of per phase timing and operational parameters in addition to the normal NEMA settings. These plans can be called by specific cycle/split combinations or by time clock circuits.

NOTE: When implemented, the service plan programming will override the normal NEMA settings, i.e. recall status, MGR, etc. Normal NEMA settings thus no longer apply for the parameters specified by service plans.

Service plans include:

Recall status--Omit, actuated, CNA, recall extendible, recall max, soft recall, ped recall, and ped omit (phase is actuated).

Min Grn--0-9.9 or 127 seconds

Passage--0-9.9 or 127 seconds

Walk--0.9.9 or 127 seconds

Ped Clear--0.9.9 or 127 seconds

Max plans include:

Normal Max--0-9.9 or 127 seconds, replaces normal max timer.

Fail Max--0-9.9 or 127 seconds, only used when the phase is placed in **"Max Fail Recall"** due to a detector failure. Normally set lower than normal max (see Detector Fail Monitoring).

Note: The when using Fail Max and Detector Fail monitoring by time of day, the Fail Max values for Max Plans corresponding to peak periods might be set closer to the normal max than those during off peak periods, which might be much lower.

OPTIONS MENU....SELECTION 5...SERV/MAX PLANS

```
      --SERV/MAX PLANS MENU--
1.SERVICE PLANS
2.MAX PLANS
```

SERVICE PLANS....SELECTION 2

```
-- SERVICE PLAN 1< -- (PGDN TO CONTINUE)
   PH    1   2   3   4   5   6   7   8
 CALL    0   0   0   0   0   0   0   0
  MGR    0   0   0   0   0   0   0   0
```

PG DWN....

```
SPl  PH  1   2   3   4   5   6   7   8
  PSG    0   0   0   0   0   0   0   0
  WLK    0   0   0   0   0   0   0   0
  PCL    0   0   0   0   0   0   0   0
```

PG DWN ETC....through service plan 8.

There are two pages to each of 8 Service Plans. Plans can be accessed by paging down in order, starting with plan 1. However, intermediate plans (screens) can be skipped over by changing the plan number on the upper left of the first page. Note that changing this number does not affect any plan data, only the screen displayed (i.e. you can jump from say plan 1 screen to plan 8).

The Service plan data is as follows:

Call status--Specify the call status for each phase:

0 = Omit
1 = Actuated
2 = Non Actuated (same operation as "CNA")
3 = Recall Extendible
4 = Recall Max
5 = Soft Recall
6 = Ped Recall
7 = Ped Omit (phase is actuated)

MGR, PSG, WLK, PCL--Load 0-9.9 or 127

Service plan parameters are implemented whenever the particular plan is, which is a function of cycle/split combinations or clock. Cycle/split selection **overrides** clock when both are selecting. Refer to the second page of the phase service run mode display for current service plan status and mode of selection (0= none, normal NEMA).

MAX PLANS.....PRIOR MENU....SELECTION 2....

```
      --MAX TIME MODE--          | 0 = NEMA
PHASE  1  2  3  4  5  6  7  8    |1= SELECT
 MODE  0  0  0  0  0  0  0  0    |   MAX BY
     --PGDN TO CONTINUE--         |TOD/COORD
```

This screen determines which phases will allow Max Plan timing. It can be programmed so that some phases allow Max Plan timing but others would remain strictly NEMA.

PG DWN....

```
          -- MAX TIME PLAN 1< --
  PHASE  1   2   3   4   5   6   7   8
NORM MX  0   0   0   0   0   0   0   0
FAIL MX  0   0   0   0   0   0   0   0
```

Each of 8 plans can be accessed by paging down in order, starting with plan 1. However, intermediate plans (screens) can be skipped over by changing the plan number at the top of the page (Enter). Note that changing this number does not affect any plan data, only the screen displayed (i.e. you can jump from plan 1 screen to plan 8).

Normal Max…0-255 seconds, replaces normal max timer when max plan is in effect.

Fail Max…0-255 seconds, only used when the phase is placed In "Max Fail Recall due to a detector failure. Normally set lower than normal max (see Detector Fail Monitoring).

DETECTORS

PRIOR MENU SELECTION 6....DETECTORS....

```
     --DETECTOR PROGRAMMING MENU—
1.MEMORY/CALL/EXTEND  3.DET FAIL MINITOR
2.DELAY/STR/DIS       4.DET SIMULATION
```

SELECTION 1....MEMORY/CALL/EXTEND

```
DET INP    1   2   3   4   5   6   7   8
MEMORY   OFF OFF OFF OFF OFF OFF OFF OFF
CALL PH    1   2   3   4   5   6   7   8
EXT/SW   1/1 2/2 3/3 4/4 5/5 6/6 7/7 8/8
```

PG DWN….detectors 9-24….

Detector programming provides phase assignable inputs, detector switching, memory on/off per input, and stretch/disconnect/delay timing.

The default settings for detectors 1-8, as shown, are for standard NEMA operation, with no switching, stretch, disconnect, or delay features programmed. The default state for detectors 9-24 is for no operation (as indicated by all 0's). The LMD units are in the default state when shipped, The controller clear code will also lead default values. The features provided are described as follows

MEMORY……This program allows memory on/off status to be assigned at the input level. It could be used in applications where on input would have memory on but another has memory off. For example, a dedicated right turn lane could have memory on-although they both call the same phase.

Note: In order to use independent memory on/off assignment at the input level, the phase level on/off status must be programmed off (the phase level is assigned from the MEMORY/RECALL/CNA menu). If program-med on at the phase level, calls will be latched regardless of the input memory status.

CALL PH…….The phase to which the input will place a call (during red). The call phase can be programmed as:

0 = No phase called by detector input

1-8 = Call phase 1-8 (1 phase per detector input)

EXT/SW……Assigns extension and switch phases. The EXT phase is extended if it is green, regardless of SW phase-if it is green or not. The SW phase is extended only if it is green and the EXT phase is not. For example:

0/0 = No Extension phase, no switch phase. May be used for "call only" detector, where a phase is assigned to call, but not extend.

1/1= Normal. Since the EXT and SW phase are the same, the detector would operate normally (NEMA).

1/6 = Extend phase 1 if phase 1 is green. Switch to phase 6 if it is green only (phase 1 is not green).

STRETCH, DISCONNECT and DELAY

PG DWN or PRIOR MENU…Selection 2….

```
DET INP   1   2   3   4   5   6   7   8
  DELAY   0   0   0   0   0   0   0   0
STR/DIS   0   0   0   0   0   0   0   0
   MODE   0   0   0   0   0   0   0   0
```

PG DWN FOR DETECTORS 9-24

DELAY…. Pertains to call phase, during red only. The detector zone must be continuously occupied during the delay period for a call to be placed on the phase (whether memory is on or off).

STRETCH…Pertains to the **EXT/SW** phase(s) during the green only. Stretches the end of the pulse by the programmed value. T

DISCONNECT….Pertains to CALL phases only, during green. The discontent timer is held at full value during green, and the input is active (low). If not active (high) the timer times down and the detector input will be effectively disconnected or unresponsive to further activity

MODE…..

0 = Normal stretch mode

1-8 = The delay timer only times if the enable phase is green. Typically used with 5 section head protected/permissive left turns on the main street to enable the delay only when in the opposite thru green (e.g. ph 2 is the enable for ph 1's delay). This prevents a resting main from immediately terminating when a left turn actuation arrives. ..yet prevents skipping a late arriving left turn when cycling around from the side street.

Note: Special logic is provided in dual ring operation so that, after the delay, **both** thru's will terminate even if returning back to just one left turn. The adjacent thru will then red-revert back to green. This is done to prevent vehicles from being trapped and for safety (since opposite turn drivers tend to assume that both sides will clear).

9 = disconnect mode

DETECTOR FAIL MONITOR

PG DWN.....or PRIOR MENU....SELECTION 3...

```
      --DET FAIL SAMPLE PERIOD--
TIME  | 0-255 MINUTES DETERMINES
  0   | PERIOD FOR DET FAIL MONITORING
        --PGDN TO CONTINUE--
```

Sets the time duration, in minutes, for the detector fail sampling period for all detectors. For example, if 10 minutes is chosen, then no activity, over/under thresholds, and constant call status will all be re-determined every ten minutes based on activity over that 10 minute interval.

DETECTOR FAIL MONITOR ENABLING

PG DWN.....detectors 1-8.....

```
        --DETECTOR FAIL MONITOR
 DET    1   2   3   4   5   6   7   8
MODE   OFF OFF OFF OFF OFF OFF OFF OFF
        --PGDN TO CONTINUE--
```

PG DWN....MSD detectors 9-24.....

This programming determines if the associated detector will be monitored. When off, no monitoring will take place.

DETECTOR MONITOR PARAMETERS...PG DWN....

DET	1	2	3	4	5	6	7	8
PHASE	0	0	0	0	0	0	0	0
MIN	0	0	0	0	0	0	0	0
MAX	0	0	0	0	0	0	0	0

PG DWN ETC....for detectors 9-24.

For each detector:

Phase--The phase to be placed in **Fail Max Recall.** Program 0 if no phase is to be placed on Max Fail Recall if the detector fails. Assign phase 1-8 if one is. **Note:** If you wish to monitor a detector in terms of logging and reporting, but do not wish to place a phase on Max Fail Recall, set the phase = 0.

Min--The minimum allowable counts over the sampling period. **Note:** a value of **0** will disable both the no activity monitor and the under threshold monitor. A value of **1** will disable the under threshold monitor, but allow the no activity monitor (counts lower than 1 would be considered "no activity"). A value greater than **2** will allow distinction between "under threshold" and "no activity" monitors (one or the other can occur, not both).

Max--Set the maximum number of allowable counts over the period. Usually used to monitor for a detector in oscillation ("chattering").

DETECTOR SIMULATION

PRIOR MENU.....Selection 4.....DETECTOR SIMULATION

```
  --DETECTOR SIMULATION MODE--
            0 = OFF
MODE:  1< 1 = INPUT and SYSTEM LEVEL
            2 = SYSTEM LEVEL ONLY
```

PG DWN.....

DET	1	2	3	4	5	6
SAT FLOW	2400	2400	1800	1800	1800	2400
PRCNT SAT	10	10	10	10	10	10
TOTAL VOL	240	240	180	180	180	240

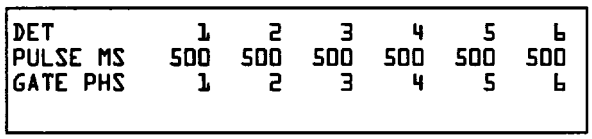
PG DWN.....for detectors 7-24....

SATURATION FLOW RATE - In vehicles per hour, during green, the number of vehicles that could pass the detector if flow was uninhibited.

PERCENT SATURATION - The percentage of the SATURATION FLOW RATE that will be used during simulated operation.

TOTAL VOLUME - This is not a programmable entry, it is a calculation of the above two entries. For example, SATURATION FLOW RATE is entered as 1,800 VPH, PERCENT SATURATION is entered as 10%, the resulting TOTAL VOLUME would be 180 VPH.

PG DWN.....for PULSE WIDTH and GATE PHASE.....



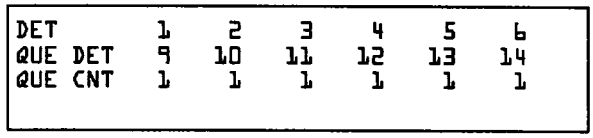
DET	1	2	3	4	5	6
PULSE MS	500	500	500	500	500	500
GATE PHS	1	2	3	4	5	6

PG DWN.....for detectors 7-24....

PULSE - The PULSE WIDTH in milliseconds of each simulated detector input. This would simulate how long (msec) the detector zone were occupied, for simulation of computed speed.

GATE PHASE - The phase or overlap, which when red, builds up simulated calls and then discharges calls (vehicles) at saturation flow rate when phase is green.

PG DWN.....for QUEUE DETECTOR AND QUEUE COUNT.....



DET	1	2	3	4	5	6
QUE DET	9	10	11	12	13	14
QUE CNT	1	1	1	1	1	1

PG DWN.....for detectors 7-24....

QUEUE DETECTOR - An upstream detector input (1-24) that would be used to count vehicles on their way to the stop bar. This detector input enters counts during red.

QUEUE COUNT - Number of calls (vehicles) counted on QUEUE DETECTOR before input reports full occupancy (steady on). The above two entries would be used to simulate ADAPTIVE SPLIT OPERATION.

SECTION V

COORDINATION PROGRAMMING

COORDINATION PROGRAMMING

Return to Program/Read mode menu...

```
          --PROGRAM/READ MODE--
1.SECURITY CODE 4.TIME CLOCK  7.REPORTS
2.CONTROLLER    5.PRE-EMPTION
3.COORDINATION  6.COMM SET-UP
```

COORDINATION....Selection 3

```
          --COORDINATION DATA---
1.COORD MODES     4.COORD PH/SERV PLANS
2.OFFSET SEEK     5.CYCLE/OFFSET LENGTHS
3.OPTIONS/L.LAG   6.FORCE OFF & PERMS
```

COORD MODES

Selection 1.....

```
              --COORD MODES--
 FL    9<|ON/OFF 9=TC 10=INT 11=COM 12=AU
SYS    9 |ON/OFF 9=TC 10=INT 11=COM 12=AU
          --PGDN TO CONTINUE--
```

PG DWN....

```
              --COORD MODES--
CYC   9<|1-8=MAN 9=TC 10=INT 11=COM 12=AU
SPL   9 |1-4=MAN 9=TC 10=INT 11=COM 12=AU
OFF   9 |0-5=MAN 9=TC 10=INT 11=COM 12=AU
```

CODES:

ON/OFF = Manually Selected/Disabled Flash, System
0-8 = Manually selected cycle, split, or offset. "0"for offset means no offset output active.
9 = Time clock mode (time base coordination)
10 = AC interconnect mode
11 = Communications (closed loop system). Clock is the back-up mode if COM fails.
12 = AUTO, i.e. clock or interconnect. Depends on the "Interconnect inhibit" input (MSD pin 37), or Clock Ckt. 54. When using the input, Low = Clock. Usually used to initiate a time clock back up for an interconnect system

Note: Clock circuit 147, *Call to Clock Mode*, is a special circuit that is more powerful than interconnect inhibit. This circuit forces time clock control for all operating parameters, regardless of their normal programming, Comm, Interconnect, etc.

OFFSET SEEKING

PRIOR MENU...Selection 2....(or PG DWN from previous)

```
          --OFFSET SEEKING MODE--
SEEKING    | 0. RESYNC    2. SHORTWAY
MODE  2<   | 1. DWELL     3. INTERRUPTER
          --PG DWN TO CONTINUE--
```

Select 1 of the 4 offset seeking modes. See Section II for offset seeking definitions.

Note that the resync mode is a manual and temporary* method of resetting the local cycle timer. When in effect, there is no offset timer, the local cycle timer is simply reset at the appropriate moment and times from that point. The cycle timer is reset from the *Coordination Timing* run mode screen by pressing the CLEAR key.

*The resync timing is lost on power outage.

COORDINATION OPTIONS

PRIOR MENU...Selection 3.....(OR PG DWN).....
OPTIONS/LEAD LAG

```
        --COORDINATION OPTIONS--
1.OPERATIONAL       3.ADAPTIVE SPLIT
2.CSO TO LEAD/LAG   4.CSO TO CKT MAPPING
```

SELECTION 1.....OPERATIONAL...

```
FLOAT IL SYNC I SYS TO  ICS0/ISCM IWALK
F.O.'SITO FREEI MX2 CNA IFREEIMODEIADJ
 OFF   I  OFF  I OFF OFF I  D  IOFF IOFF
```

FLOATING FORCE OFFS

ON=Each coordination force off value becomes a green time based on the beginning of the associated green rather than a fixed force off point. Thus, when enabled, force offs are programmed as *green times,* not as fixed positions In the cycle. Permissives are programmed normally.

Note: When this mode is enabled, permissives are the only parameters that link the controller phasing to the back-ground cycle. The effect of Floating force offs is that non-coordinated phases cannot receive more green time than allocated because the force off timing begins with green--even if the phase begins early. Only the coordinated phase(s) can get extra green time because hold is applied until the yield point (permissive) arrives.

OFF = Coordination force offs are fixed. In the fixed force off mode, an early starting phase can extend up to its force off point--which remains fixed to the cycle—thus allowing more green time if the phase starts as a result of a previous phase being skipped or gapping out early

3 = Special code. Coordination force offs are fixed, but force offs are inhibited on CNA phases.

Note: Floating vs. fixed force offs is a matter of preference. The argument for fixed force it that it is more efficient to let the total cycle green time be spread out among those phases that have the demand. Max time restrictions can be placed to prevent extremes. The argument for floating force offs is that no extra green time can go to any but the coordinated phase(s).

LOSS SYNC TO FREE:

ON= Unit goes free if sync pulses are lost
OFF= Unit stays in sync based on internal timing

SYSTEM TO MX2:

ON= MX2 called when in system mode
OFF= No call for MX2

SYSTEM TO CNA:

ON = CNA applied to the active coordinated phases
OFF = No call for CNA

CSO/FREE OPERATION

0 = No combination of CIS/O to free operation.

111-956= Specifies a combination of C/SIO that, when called for, will cause the unit to go to free operation. 9 is the "don't care" state for cycle, 5 =split, and 6 = offset.

HOLD OUT: The hold out function is not present in this screen because the LMD9200 has general I/O mapping. The hold out function still exists, however, and can be mapped to any pin by assignment in the I/O Configuration Menu, Output Mapping, page down four times (HOLD). The LMD8000 had allowed an option to assign hold out to MSD pin 48 or MSA pin d (phase 2 check). In the LMD9200 these are equivalent to I/O mapping codes 448 and 127 respectively. Be sure to zero out the normal function (such as assign 0 to phase 2 check) before assigning hold out to a pin.

SCM (Subordinated Coordination Mode):

When SCM is ON, the LMD9200 will tolerate over-timing of "non-forcible phases during coordination by stopping the cycle timer until a phase can force off. This prevents skipping or short timing later phases. Over-timing can occur for a number of reasons, often due to actuated peds that are seldomly used and thus do not warrant normal split timing. When over-timing occurs, the cycle timer will be out of sync, but will re-sync smoothly by normal offset seeking.

WALK ADJ (Walk adjust)

When WALK ADJ is ON the LMD9200 will shorten the timing of a walk if it determines that the phase is not going to be able to force off due to ped timing. It is typically used in urban settings where peds "fill up" the split and shortway offset seeking is used. A walk can then be shortened as necessary to as low as 10 seconds. This allows shortway offset seeking to force off a phase earlier when it is trying to shorten the cycle. Otherwise the cycle can get out of sync with the phases because they cannot force off (also see SCM).

C/S/O TO LEAD/LAG SEQUENCES

PG DWN (From coord options screen)

```
          --LEAD LAG PATTERNS--
SEQ  CSO  1&2  3&4 5&6 7&8 I  1= ODD LEADS
 1   946   2    1   1   1  I  2= ODD LAGS
          --PGDN TO CONTINUE--
```

PG DWN, ETC....through SEQ 10

Each sequence is related to a selected pattern of cycle, split, and offset. If that CSO pattern becomes active, certain phase pairs may become lead/lag phases, where "1" is the normal sequence and "2" reverses the phases. When reversed, the odd phase follows the even phase. Note that a "9" for cycle, a "5" for a split or a "6" for offset is the "don't care" state. In the above example, split 4 with any combination of cycle or offset will lag phase 1.

Also note that the controller must be programmed (under controller sequence menu) for “Lead Lag Mode” and “Auto” for any pairs to be lagged by CSO.

ADAPATIVE SPLIT CONTROL

Adaptive split control is a means of selecting splits based on local demand. Adaptive split is enabled by clock CKT 109, thus, it can be enabled by time of day or full time (CKT 109 on). The coord “split mode” would be programmed normally for any of the other modes (TC, COM, etc.).

There are two *modes* of adaptive split selection, one is based on the amount of force offs on selective phases, the other is based on Queues. Queues are determined by set-back detectors with delay times. If the delay times out, a queue count is registered. A detector is recognized as a queue detector by assignment to phases under “Q DET” programming in this section.

SELECTION 3…ADAPTIVE SPLIT CONTROL…

```
       -ADAPTIVE SPLIT SELECTION-
CYCLES  0<|  NUMBER CYCLES PER SAMPLE
MODE    0  |  0= QUEUES, 1= FORCE OFFS
THRSH   0  |  MIN. # Q'S/F.O. 'S TO SELECT
```

PG DWN…

```
SPL/PH 1 2 3 4 5 6 7 8 |
 1     0 0 0 0 0 0 0 0 | 0=NOT CONSIDERED
 2     0 0 0 0 0 0 0 0 | 1=SELECTED PH'S
     --PGDN TO CONTINUE--
```

PG DWN…

```
SPL/PH 1 2 3 4 5 6 7 8 |
 3     0 0 0 0 0 0 0 0 | 0=NOT CONSIDERED
 4     0 0 0 0 0 0 0 0 | 1=SELECTED PH'S
     --PGDN TO CONTINUE--
```

PG DWN…

```
--QUEUE   DET   TO   PHASE    ASSIGNMENT-
 PHASE   1   1   2    2    3    3    4   4
 Q DET   0   0   0    0    0    0    0   0
Q DELAY  0   0   0    0    0    0    0   0
```

Q DET = detector 1-24
Q DELAY = 0 – 9.9 or 0-127 seconds

PG DWN FOR PHASES 5-8

Adaptive split operation

Each split is assigned a set of selective phases. These are phases that apply to the selection of that split. The base period is determined by the sample number of cycles (starts/ends at cycle zero). The total number of force off’s or Queues is determined for each split over the sample number of cycles. For example, say the force off mode is used, and split 2’s selective phases are 3 and 7. Now, say that over the sample number of cycles, 3 forced off once and 7 forced off twice. The total for split 2 would then be 3.

Starting from split 1, the split with the highest total exceeding the minimum threshold is selected for the duration of the next sampling period. The LMD will remain in the selected split until a new split with a higher number of force offs or Q’s exceeding threshold occurs. If two splits have the same number of F.O.’s or Q’s, then the lower numbered split will be selected. For semi-actuated applications, assign 0’s to split 1 and let other splits be selected based on *exceeding the threshold*. The LMD will default to split 1 if not exceeded in this mode.

If used, queues are based on the Q detector programming. Each phase is assigned up to 2 Q detectors (1-24) with delay periods. The delay timer times down when the detector is active, and sets to full value when inactive. If the detector is active for the entire delay period, a queue is registered for that phase. Detectors 1-24 can be used as queue detectors. Normal calls, extensions, or standard detector stretch and delay timing are not affected.

Adaptive split inhibits

Page down from the Q detector to phase assignments to get the adaptive split inhibits screens. For each cycle, specify which, if any, split will be inhibited from auto selection in relation to specific combinations of cycle and offset.

CSO TO CIRCUIT MAPPING

PRIOR MENU to OPTIONS MENU…. Selection 4…. CSO TO CKT MAPPING

```
    --CSO TO TIME CLOCK CKT MAPPING—
CSO/S CKT CKT CKT CKT CKT CKT CKT CKT
000/0   0   0   0   0   0   0   0   0
000/0   0   0   0   0   0   0   0   0
```

PG DWN ETC…through **C/S/O** page 5, combinations 9 & 10. Any of the available Time Clock Circuits can be activated by selected combinations of cycle, split, offset, and/or system. Specify desired C/S/O with system/no system along with any time clock circuits to be active. Enter the time clock circuit number under **"CKT"** (up to 8 circuits per **C/S/O** combination. 9, 5 ,6= Don't care states for C/S/O. 0**=** don't care state for system, 1= in system only, 2= not in system only. For example, to inhibit MAX timing during system operation, program C/S/O combination 1; 956/1 and the first two CKT columns 15 and 16 respectively. Inhibit MAX timing will occur for any C/S/O combination when in system operation.

COORD PH/SERV PLANS

PRIOR MENU ....Selection 4....**COORD PH/SERV PLANS**

```
 CYC/SP  C1 S1 S2 S3 S4 |C2 S1 S2 S3 S4
COORD PH'S  26 26 26 26 |   26 26 26 26
SERVICE PL   0  0  0  0 |    0  0  0  0
MAX PL       0  0  0  0 |    0  0  0  0
```

PG DWN ETC...through Cycle 7&8. Each of 8 cycles can be accessed by paging down In order, starting with cycle 1&2 as above. Intermediate cycle screens can be skipped by changing the cycle number at the top of left of the page (select cycle 1, 3, 5, 7 then Enter). Note that changing this number does not affect any data, only the screen displayed (i.e. Jump from cycle 1&2 screen to cycle 7&8).

Each screen specifies the following:

Coord ph's. Specifies the coordinated phases for that cycle/split combination. The first digit is the ring 1 phase and the second is the ring 2 phase. Load the second digit as a 0 if single ring (eg. 10 = phase 1, ring 1). Note that the force off and permissive programming for the specified cycle and split must be consistent with the coord phases

Service plan. Specifies the service plan 0-8 (0= none) to be implemented with that cycle/split (see service plans).

Max plan. Specifies the max plan 0-8 (0= none) to be implemented with that cycle/split (see max plans).

Notes:

1.Program 0's If you do not wish to use service/max plans or If you wish to select them strictly by clock circuit. Cycle/Split (C/S) selection of service and max ***plans will override time clock*** when both are active.

2. Prior to Rev 7, the LMD8000 did not have to be "in system" for cycle/split selection of a service and/or max plan... only that the specific cycle/split Is selected. From LMD8000 rev 7 and higher (and all 9200 versions), "system" *must be active* (coordinating). Thus, the unit will automatically revert to Clock selection or normal NEMA values when not in system. Prior to rev 7 this required a return to a "dummy" cycle and split with 0's for service and/or max plans when In free operation.

CYCLE LENGTHS AND MAX DWELLS

PG DWN OR SELECTION 5....

```
          --CYCLE LENGTHS—
 CYCLE   1   2   3   4   5   6   7   8
LENGTH  90 100 110 120 120 120 120 120
MAX DWL 30  30  30  30  30  30  30  30
```

Sets Cycle Lengths and Max Dwell values (0-255 secs).

Max Dwell is a setting used with Dwell mode offset seeking, restricting the amount the unit can dwelt In any one cycle (typically set 20-35% of cycle length).

OFFSET TIMES

PG DW1 from cycle lengths...

```
      --OFFSET TIMES  (0-255 SECS)--
       OFF 1  OFF 2  OFF 3  OFF 4  OFF 5
CYC 1     0      0      0      0      0
CYC 2     0      0      0      0      0
```

PG DWN ETC...through cycle 7 & 8.

FORCE OFFS AND PERMISSIVES

PRIOR MENU....Selection 6...FORCE OFF + PERMS

```
      --FORCE OFFS & PERMISSIVES-
1.  READ OR MANUALLY LOAD
2. AUTO CALCULATE FROM PERCENTS
```

NOTE; If the Auto calculate option is selected, Associations, Force offs, and Permissives will be calculated from percentages, and need not be manually programmed.

READ OR MANUALLY LOAD

Use this option if you wish to view data previously loaded (including auto-calculated values) or wish to manually load.

```
     --FORCE OFFS & PERMISSIVES--
1.PED PERM/PERM MODE     3. PERMISSIVES
2.FORCE OFFS
```

PED PERMISSIVES/PERMISSIVE MODE....Selection 1

```
  --PED PERMISSIVE TIME/PERM MODE--
PED PERM|1-255=SECS.|PERM MODE|0=STD
   0    |0= AUTOCALC|    0     |1=STRICT
         --PGDN TO CONTINUE--
```

The ped permissive provides an independent permissive timing period for ped timing--which usually requires more guaranteed time than the vehicle. The ped permissive operates in conjunction with the vehicle permissive for each phase. It begins timing with the vehicle permissive, but then times independently based on the ped perm value.

For example, say the ped permissive is set at 10 and a given vehicle permissive starts at 7 and ends at 25. The ped permissive would then time from 7 to 17. From 17 to 25 vehicles would be permitted only.

Ped Perm = 0 is a special case in which the ped permissive is calculated *automatically for each phase* from vehicle permissives. In this case, the ped permissive also begins with the vehicle permissive but ends [(WLK + PED CLR) - MGR] seconds prior to the end of the vehicle permissive. If minimum green is greater than walk + ped clearance, the ped permissive ends with the vehicle permissive. The ped permissive will be assigned a minimum of 1 second regardless of the calculation. **Any other** non-zero value sets a ped perm value, which starts at the beginning of the vehicle permissive and ends when the specified value expires (one value for all peds).

Strict Permissives are an optional permissive mode where the permissive periods are not conditioned by the coordinated phase as are normal LMD permissives. Normally, after leaving the coordinated phase, all phase omits are released thereby allowing all non-coordinated phases in order. Strict permissives only release phase omits when scheduled to do so, regardless of phase.

FORCE OFF ASSOCIATIONS

PG DWN OR Selection 2...FORCE OFFS

```
    --FORCE OFF ASSOCIATIONS--
F.O.     1  2  3  4  5  6  7  8
PHASE(S) 1  2  3  4  5  6  7  8
         --PGDN TO CONTINUE--
```

Assigns phases to force offs, up to 2 phases per force off. Only phases assigned to a force off will be forced off at the time of occurrence (see next screen).

Note: If the automatic calculation of force offs and permissives is chosen, then force offs will automatically be assigned; F.O # 1 = phase 1, F.O # 2 = phase 2, etc.

FORCE OFF TIMES

PG DWN....Force off timings.....

```
 --CYCLE 1<SPLIT 1 FORCE OFF TIMES--
F.O.   1  2  3  4  5  6  7  8
TIME   0  0  0  0  0  0  0  0
         --PGDN TO CONTINUE--
```

PG DWN

```
 --CYCLE 1<SPLIT 2 FORCE OFF TIMES--
F.O.   1  2  3  4  5  6  7  8
TIME   0  0  0  0  0  0  0  0
         --PGDN TO CONTINUE--
```

PG DWN ETC...through cycle 8 split 4

Specify a time value, in seconds, for each force off in each cycle and split. **Review coordination options page 2-11.**

Note that the curser can be located on the cycle and split numbers as well as the force off data fields. This allows the scre en to be "jumped" ahead (key the desired cycle and split in these positions--data is not altered).

Note: if the auto-calculate option is chosen, force off times will be automatically calculated from percentages, and need not be manually programmed.

PERMISSIVES

PG DWN, or PRIOR MENU...PERMISSIVES

```
    --PERMISSIVE ASSOCIATIONS--
PERM 1       2        3        4
PHS 1        2        3        4
        --PGDN TO CONTINUE--
```

PG DWN

```
    --PERMISSIVE ASSOCIATIONS--
PERM 5       6        7        8
PHS 5        6        7        8
        --PGDN TO CONTINUE--
```

Specifies what phases will be assigned to each permissive. Each permissive can be assigned 1 or up to 8 phases.

Review pages 2-11through 2-14 for permissive operation.

Note that for purposes of observing permissives on the coordination timing display, it makes sense to assign phase 1 to perm 1, phase 2 to perm 2, etc. In this way the permissives on the run mode screen will represent the phases directly (the back-up plans all use this technique).

Note: If the automatic calculation option is chosen, then permissives will automatically be assigned; Perm # 1 = phase 1, Perm# 2 = phase 2, etc.

START AND END PERMISSIVES

PG DWN....Start and end of permissives....

```
 --CYCLE 1 SPLIT 1 PERMISSIVE TIMES--
PERM    1   2   3   4   5   6   7   8
START   0   0   0   0   0   0   0   0
END     0   0   0   0   0   0   0   0
```

PG DWN....

```
 --CYCLE 1 SPLIT 2 PERMISSIVE TIMES--
PERM    1   2   3   4   5   6   7   8
START   0   0   0   0   0   0   0   0
END     0   0   0   0   0   0   0   0
```

PG DWN ETC....through cycle 8, split 4

For each permissive, specify a start and end time, in seconds, from 0-255. Review Section II for details on permissives operation.

Note that, as with force off screens, the cycle and split numbers can be entered to switch screens without paging down (or up). This does not change data but can quickly change screens--such as from cycle 1 split 1 to cycle 8 split 4 by entering 4 for cycle and 4 for split.

Note: if the auto-calculate option is chosen, permissive times will be automatically calculated from percentages, and need not be manually programmed.

AUTO-CALCULATE FORCE OFF's & PERMS

The LMD can automatically calculate force offs and permissives internally from user entered percentage values.

Before even entering autocalc:

1. Be sure the controller is otherwise **fully programmed.** Much of the auto-calc process is based on other controller settings (sequence, phases used, MGR, YEL ,RED, Walk, PCL, etc.).

2. All other **COORD DATA** should be programmed as well, including COORD MODES, OFFSET SEEKING MODE, OFFSETS, CYCLE LENGTHS, COORDINATED PHASES, etc.

3. Keep in mind that auto-calc will take into account and *automatically compensate* for any Cycle/Split with a **Service Plan** (which might have different MGR, WLK or PCL values) or Lead/Lag reversal assigned. Again, program these items first.

4. The **minimum percentage** required for each phase (see error screens) includes WLK + PCL timing. If it is desired that such timing not be taken into account, set the ped timing to zero, run autocalc, then re-program the ped timing. Note that if this is done, a ped call on such a phase *may* result in a late return to the coord phase. This may be acceptable if the ped is seldomly used.

5. **"Floating force offs"** is a controller option that bases force offs on a green time value started at the beginning of green of each phase. This is opposed to the normal **"fixed force offs"** which have a designated point in the cycle. When the Floating Force Offs mode is selected (ON), the auto-calculation will adjust for this and load force offs as green times. The permissives will be the same as for fixed force offs.

LOADING SET-UP DATA FOR AUTO-CALC

Before actually running auto-calc, basic phase percentages and other set-up information must be specified. To do this, enter the auto-calc menu:

PROGRAM/READ–COORDINATION–FORCE OFF & PERMS...

```
     --FORCE OFFS & PERMISSIVES--
1.READ OR MANUALLY LOAD
2.AUTO CALCULATE FROM PERCENTS
```

Selection 2...AUTO-CALCULATE FROM PERCENTS....

```
    --AUTO CALCULATE FO/PERM MENU--
1.SPLIT PERCENTS     3.NORMAL/CNA
2.PERMISSIVE TYPE    4.RUN AUTO CALC
```

SPLIT PERCENTS

The phase split percentage values are loaded in this section prior to running the auto-calculation routine.

SELECTION 1....

```
        --SPLIT PERCENTS MENU--
1.LOAD SPLIT PERCENTS
2.COPY 2-8 PERCENTS FROM CYCLE 1/SPL 1-4
(BE SURE TO LOAD CYCLE 1 PERCENTS FIRST)
```

LOAD SPLIT PERCENTS...SELECTION 1.....

```
       --CYCLE 1< SPLIT PERCENTS--
PHASE    1  2  3  4  5  6  7  8 | R1  R2
SPLIT 1  0  0  0  0  0  0  0  0 |  0   0
SPLIT 2  0  0  0  0  0  0  0  0 |  0   0
```

PG DWN...(splits 3&4)

```
       --CYCLE 1< SPLIT PERCENTS--
PHASE    1  2  3  4  5  6  7  8 | R1  R2
SPLIT 3  0  0  0  0  0  0  0  0 |  0   0
SPLIT 4  0  0  0  0  0  0  0  0 |  0   0
```

PG DWN, ETC. THROUGH CYCLE 8 SPLIT 4.

The data is entered in terms of the percent allocation to each phase. The percentage is total phase time, including clearances, not just green time. The total column keeps a running tab of percent sums by ring as each entry is made.

COPY CODES

If the copy codes are desired, first load all 4 splits into cycle 1. These percentages can then be copied to Cycle 2-8. See the "Error Displays" section for rules on acceptable percentage values.

PERMISSIVE TYPE

This section will define how the LMD will calculate permissives. There are some options available.

```
--PERMISSIVE TYPE--
TYPE  0<|0=YIELD, 1=SINGLE, 2=MULTIPLE
MODE  0 |0/1=START/END COORD PH AT CYC 0
EGB%  0 |0-99% = COORD PH EXT GRN BAND %
```

PERMISSIVE TYPE DEFINITIONS

0= YIELD. A 5 second permissive is extended to all phases from the coordinated phase force off.

1= SINGLE. The first permissive starts at the coordinated phase force off but includes only the first set of phases immediately following the coordinated phase (say 3 and 7 in a NEMA dual ring 8 phase sequence). This permissive ends enough before the associated force off points (for 3 and 7) to allow for clearing the coord phase and timing min green. The next permissive (say to 4 and 8) starts at the first phase (3 and 7) force off point and ends appropriately before the its force off(s). Use this method if you wish to stay in coord phase green after the yield point if no calls are present on the first group (3 & 7). This prevents the second group (4 and 8) from starting much too early, plus gives a "window" to the first group (3 & 7) for late arrivals.

2= MULTIPLE. All permissives start at the coordinated phase force off (allowing all phases). Each permissive ends enough before its associated phase force off point to allow for clearing the coord phase and timing min grn. Use this method if it is okay for downstream phases to start early if no demand on earlier phases.

PERMISSIVE TYPE NOTE: The above descriptions refer to **"starting the first permissive at the coordinated phase force off point"**. Permissives may Actually start *earlier* than that if the extendible green band method is used (see EGB% description).

MODE

0= START. Force offs and permissives will be calculated such that the coordinated phase (main street) green will start at cycle 0.

1= END. Force offs and permissives will be calculated such that the coordinated phase (main street) green will end at cycle 0.

MODE NOTE: The LMD references offsets to cycle 0 regardless of the phase(s) active at that point. Thus, offsets reference to the *beginning* of main street green when in mode 0 and the *end* of MSG in mode 1.

EGB% (EXTENDIBLE GREEN BAND %)

EGB%: 0-99% This is the percentage before the coordinated phase force off to start the first permissive(s). E.g. if the coordinated phase force off is calculated to be 40 seconds into a given cycle and the EGB% is 50, then the first permissives will start 50% earlier, or at 20.

EGB% Concept: Allows a variable green band on the coordinated phase in fully actuated applications. Regardless of demand, the coordinated phase will hold until the first permissive begins. By starting the first permissive early, the coordinated phase can gap-out earlier, but will not force off until the scheduled force off point. This allows a variable green band on the coordinated phase based on demand.

EGB% Rules:

1. Must be fully actuated, i.e. detectors on the main street.

2. Must use Mode 0 = start coord phase at zero. The first permissive cannot start in the previous cycle. Since the LMD always references offsets to cycle zero, the offset will be referenced to the beginning of main street green (MSG) in this mode. If the offset is *supposed* to be referenced to *the end* of main street green, you must convert the end of MSG offset to the beginning of MSG by the relationship:

Beg MSG offset = End MSG offset - True End MSG

If positive, use the value directly as the offset

If negative, add the negative value to the cycle length

EXAMPLE of offset conversion: End of MSG to Beginning of MSG: Say the desired End-of-MSG-Offset is 24. However, also say this point is not zero since the controller calculates the MSG force off (End of MSG) to be 40. Say the cycle length is 90. Then:

Beg MSG offset = 24-40

= -16 (add negative value to 90)

= 74 (use this as the offset for that plan)

3. The CNA mode cannot be used on the coord phases when using a non-zero EGB%.

Use EGB% = 0 if the above rules are not met or EGB operation not desired.

NORMAL OR CNA

In this section it is specified whether the coordinated phase will operate in the CNA mode or not.

PRIOR MENU...SELECTION 3...NORMAL/CNA

```
   --NORMAL/CNA OPTION FOR AUTOCALC--
MODE  |
  0<  |0=NORMAL, NO CNA
      |1=CNA WILL BE USED ON COORD PH'S
```

Assign 0= NORMAL if the coordinated phase will operate in any other recall mode besides CNA.

Assign 1= CNA if CNA is to be used on the coordinated phase during coordination. The LMD will calculate force offs & perms differently if CNA is to be used to compensate for the fact that the coord phase will hold and rest at the end of Walk.

RUN AUTO-CALC

This is the section in which auto-calc is actually run. Be sure all other set-up vales are loaded (see the beginning of this section).

PRIOR MENU....SELECTION 4...RUN AUTO CALCULATE...

```
   --RUN AUTO CALCULATE MENU--
1. CYCLE 1 4. CYCLE 4 7. CYCLE 7
2. CYCLE 2 5. CYCLE 5 8. CYCLE 8
3. CYCLE 3 6. CYCLE 6 9. ALL CYCLES
```

Press the desired digit 1-9; the force offs and permissive values will be calculated. Be sure the controller is otherwise fully programmed and the auto-calc percentages and set-up data have been set. Auto-calc will set all permissives and force offs to zero for cycles with zero lengths.

One cycle at a time or all cycles can be calculated. Use one cycle at a time if you are changing set-up parameters per cycle.

```
CALCULATING FORCE OFFS AND PERMISSIVES
     FOR CYCLE X
```

The auto-calculation process only takes a few seconds (if no errors). Return to and select the READ OR MANUALLY LOAD option to view or edit force offs and permissives.

NOTE: The auto-calc process operates on the force off and permissives data values. You may still access and edit those force off and permissive values after the auto-calculation process has been executed.

AUTO-CALCULATION ERROR DISPLAYS

The auto-calculation process is quite rapid if the LMD detects no errors. However, if there is an error in percentage allocation or other set-up mismatch, one of the following error displays will appear. If an error code appears, go back and make the appropriate correction as suggested by the error display, then run auto-calc again.

PERCENTAGES DO NOT ADD UP TO 100%

```
--AUTO CALCULATION ERROR DISPLAY--
PERCENT VALUES CXSY DO NOT ADD UP TO
100% IN EACH USED RING. RELOAD PERCENTS
    --HIT PRIOR MENU TO EXIT--
```

Assigned percentages must add up to 100% for each used ring. The erroneous cycle and split are indicated.

NOTE: For 5 phase applications use :

1 2 | 4

5 6 | 8

Instead of:

1 2 | 4

5 6 |

This will insure 100% totals in both rings. Assign phase 8= ON prior to auto-calc even if you don't intend to use it. Program phase 8 with the exact same percentage as phase 4. Go back and program phase 8= OFF after auto-calc if you wish, although it really won't affect operation even if left on.

DUAL RING PERCENTAGE VIOLATION

```
--AUTO CALCULATION ERROR DISPLAY--
DUAL RING PERCENT VIOLATION CXSY. SUM
OF 1+2 MUST = 5+6, SUM OF 3+4 MUST = 7+8
     --HIT PRIOR MENU TO EXIT--
```

The sum of phase percentages must be logical with respect to the opposite ring and their relationship to the barrier.

MINIMUM PERCENTAGE VIOLATION

```
--AUTO CALCULATION ERROR DISPLAY--
PERCENT VALUE VIOLATION CXSY. PHASE X
NEEDS MIN OF XY% FOR MIN GRN & CLEARANCE
     --HIT PRIOR MENU TO EXIT--
```

Each phase must be allocated a sufficient percentage to allow for minimum green and clearances. If not, the error screen will indicate what that minimum requirement is.

Note that "minimum green" is actually the greater of the phase minimum green setting or the sum of WLK + PCL. If it is desired that ped timing not be taken into account for a given phase, set the ped timing to zero, run auto-calc, then re-program the ped timing. Note that if this is done and in operation, a ped call on such a phase may result in a late return to the coord phase. This may be acceptable if the ped is seldomly used.

EXTENDED GREEN BAND ERROR (EGB%)

```
--AUTO CALCULATION ERROR DISPLAY--
EGB% CAN ONLY BE NON-ZERO IF IN NORMAL
MODE AND COORD PHASES START AT ZERO.
     --HIT PRIOR MENU TO EXIT--
```

If you have made this error, you may need to review the EGB% concept. A non-zero EGB% can only be used if the coord phases are actuated (not CNA mode) and the green starts at zero (cannot start permissives before zero).

SEQUENCES VIOLATION

```
--AUTO CALCULATION ERROR DISPLAY--
AUTO CALCULATION DOES NOT OPERATE ON
SPECIAL SEQUENCES--HAND CALCULATE ONLY
   --HIT PRIOR MENU TO EXIT--
```

The auto-calculation process only operates on SEQUENTIAL, NEMA DUAL RING, and LEAD/LAG sequences. Force offs and permissives for special sequences must be manually entered.

COORDINATED PHASES VIOLATION

```
--AUTO CALCULATION ERROR DISPLAY--
INCOMPATIBLE OR NO COORDINATION PHASES
PROGRAMMED FOR CYCLE X, SPLIT Y.
     --HIT PRIOR MENU TO EXIT--
```

OR....

```
--AUTO CALCULATION ERROR DISPLAY--
1 COORD PHASE FOR SEQUENTIAL, 2 COORD
PHASES FOR DUAL RING, CYCLE X, SPLIT Y.
    --HIT PRIOR MENU TO EXIT--
```

For all non-zero cycle lengths for which auto-calc is run, each cycle/split combination must have one coordinated phase assigned for sequential operation or two compatible phases (allowed to time together) for dual ring.

These are assigned in the coordination section under COORD PHASE/SERV PLANS in the COORDINATION DATA menu screen.

SECTION VI

TIME CLOCK PROGRAM/READ MODE

TIME CLOCK PROGRAMMING

Back to PROGRAM/READ Menu....

```
        --PROGRAM/READ MODE--
1.SECURITY CODE 4.TIME CLOCK  7.REPORTS
2.CONTROLLER    5.PRE-EMPTION
3.COORDINATION  6.COMM SET-UP
```

Selection 4.....**TIME CLOCK**

```
          --TIME CLOCK DATA--
1.UPDATE        4.EXCEPT DAYS 7.YEAR PROG
2.DLS/RES/CRD   5.CKT MODE    8. DAY PROGS
3.SYNC REF.     6.WEEK PROG   9. TIME SET
```

Selection 1....**UPDATE**

The time clock events are dependent on past and present programming. Also, the cycle sync pulses are referenced to midnight or other specific time of day. Thus, to be sure that the clock events and sync pulses are "caught up" to the present time, the "update" routine is provided....

```
    --HIT ENTER TO UPDATE EVENTS--

   HIT PRIOR MENU TO GO BACK 1 MENU
HIT MAIN MENU TO GO BACK TO MAIN MENU
```

Upon pressing the ENTER key, the LMD will enter the update routine. During this process the first line will disappear and second line of the screen will display:

```
TIME CLOCK EVENTS UPDATING
```

This line will be maintained until completion of the update routine–which may take several minutes. The controller and keyboard will operate normally during the update routine. Upon update completion, the second line will disappear and the LMD will be updated to the current time.

Note: The display may indicate that you need to load the current year and date. Do so if required.

DAYLIGHT SAVINGS, CLOCK RESET, COORD CKTs

PRIOR MENU...Selection 2...

```
    --DLS/CLOCK RESET TIME/MSD--
DLS(ON/OFF)  CLOCK RESET TIME COORD-CKTS
   ON           --:--:--            0
         --PGDN TO CONTINUE--
```

DLS = Daylight savings mode:

- On = will automatically adjust forward 1 hour at 2:00 AM on the 1st Sunday in April and back 1 hour on the last Sunday in October.
- Off = no daylight savings adjustment.

The Clock Reset time specifies the time to which the *clock will be reset* when the clock *reset input* is toggled **Note** that this has nothing to do with sync reference mode, do not confuse the two.

The COORD-CKTS specifies which coordination commands will be active on DC coordination outputs.

- 0 = Follows internal Time Clock commands
- 1 = Follows active coordination commands (system or internal)

SYNC REFERENCE MODE

PG DWN or PRIOR MENU...Selection 3...SYNC REF.

```
          --SYNC REF MODE--
MODE | 1.END OF PREV. CYCLE  3.ABSOLUTE
  2  | 2.8 INDEPENDENT       4.EVENT
       --PGDN TO CONTINUE--
```

Specify 1 of the 4 sync reference modes for time based coordination. Be sure that all units in the system have the **same** reference mode. Review the sync reference descriptions on pages 2-20 and 2-21 for more details.

Note that if modes 1 or 4 are chosen, there are no more sync reference screens. However, if the **8 independent** method is used, then.....PG DWN.....

```
  --8 INDEPENDENT CYCLE ZERO TIMES--
C1 00:00:00  C2 00:00:00  C3 00:00:00
C4 00:00:00  C5 00:00:00  C6 00:00:00
C7 00:00:00  C8 00:00:00    --PGDN--
```

These are the daily cycle zero reference times for each cycle. Midnight is the most common (and is the default) reference time. Each cycle will be independently referenced to the time specified.

If the **absolute** method used, then....PG DWN.....

```
      -- ABSOLUTE CYCLE RESET--
TO RESET CYCLE: 1 2 3 4 5 6 7 8 ALL 8:
   DEPRESS KEY: 1 2 3 4 5 6 7 8   9
  CURRENT TIME: 10:23:44      --PGDN--
```

The absolute method is a one-time (not once per day) reference, often used to sync with free running dials, or in "**City Zero**" systems. Each cycle (or all 8 at once) is manually referenced by the operator at the precise time, and runs continuously from that point–like a free running dial. After power outage, the cycle timers reference back, up to 100 hours, and "pick up" at a point in sync with a free running dial, as if power had never been out.

Each cycle timer is set (or all 8 at once) at the moment the indicated key is pressed. The current time is displayed so that the entry can be made at the appropriate moment. The cycle timers will run continuously from (and reference back to) this point without daily reference.

EXCEPTION DAYS

PG DWN or PRIOR MENU....Selection 4....EXCEPT DAYS

```
          --EXCEPTION DAYS--
EX.DAY| DOW WOM--OR DOM | MOY |DAY PROG
  1   |               1 |   1 |    2
        --PGDN TO CONTINUE--
```

Up to 35 Exception Days provide the ability to override the normally assigned day program on specific days of the year, assigning a different day program. To do so, specify the time of year and the day program which will override the normal day program on that day (only overrides that one day).

Note that there are two types of exception days:

DOW WOM MOY. This stands for Day of Week, Week of Month, Month of Year. This method would be used for day of week/week of month specific exception days. For example, Thanksgiving in Canada is the 2nd Monday in October (DOW= 2*, WOM = 2, MOY = 10). In the U.S., Thanksgiving is the 4th Thursday in November (DOW= 5*, WOM = 4, MOY = 11). Using this method, these holidays, which may fall on different dates from year to year, can be accommodated with a one time setting which is good for any year. **Use Week of Month = 5 for any DOW/WOM exception day which is the last week of the month.**

* Sunday is always day # 1 of the week.

DOM MOY. This stands for Day of Month, Month of year, i.e. the *date* 1-31. This method would be used for date specific exception days. For example, Christmas is DEC 25 (DOM = 25, MOY = 12).

EXCEPTION DAYS EXAMPLES

The following examples would be the first two exception days in many U.S. applications.

```
          --EXCEPTION DAYS--
EX.DAY| DOW WOM--OR DOM | MOY |DAY PROG
  1   |               1 |   1 |    2
        --PGDN TO CONTINUE--
```

PG DWN

```
          --EXCEPTION DAYS--
EX.DAY| DOW WOM--OR DOM | MOY |DAY PROG
  2   |  2   5          |   5 |    2
        --PGDN TO CONTINUE--
```

The first exception day represents New Year's Day, which is obviously date specific and is the 1st day of the 1st month (January 1).

The second exception day is Memorial Day (in the U.S.), which is the last Monday in May. This exception day is therefore a DOW WOM exception day. Note that Monday is "day 2" of the week (Sunday is day 1), and "5" is always used to represent the **last** week of a month.

CIRCUIT MODE

The LMD from revision 4 and higher has a greatly expanded time clock capability. From the original 13 clock ckts, the LMD now has well over 100 functions that can be controlled by internal clock. Most of these have no associated output, but provide internal control only.

Each function can be operated as ON (the function always enabled), OFF (always off), or AUTO (the function is controlled by time of day event programming). Check the clock circuit descriptions for a listing of circuit functions.

PG DWN or PRIOR MENU...Selection 5...circuit mode

```
-TIME CLOCK CKT MODE--ON,OFF, OR AU(TOD)
  CKT     8   9  10  11  12  13  14  15
FUNCT   FL  AX1 AX2 AX3 AX4 SYS MX2 IM1
 MODE  N/A  AU  AU  AU  AU N/A  AU  AU
```

For each, specify the circuit mode where:

ON = Circuit always on

OFF = Circuit always off

AU = Auto, circuit controlled by time clock events

The following are general purpose circuit outputs and are available on MSD, where:

CKT 9 = AUX 1 = MSD pin 50

CKT 10= AUX 2 = MSD pin 51

CKT 11= AUX 3 = MSD pin 52

CKT 12= AUX 4 = MSD pin 53

Note: CKT 8 and 13 are shown as "N/A". This is to indicate that they are not programmed here, but in the **"CO-ORD MODES"** section in the coordination menu.

CONTINUE PAGING DOWN....through CKT 150

CLOCK CKT DESCRIPTION

The Following chart defines the function of each of the LMD clock ckts. Recall that these can be time of day activated by programming them in the auto mode and assigning events to the day program, or, they can be full time activated by programming the circuit manually on.

CKT	ABBREV.	FUNCTION
8	FL	Flash--see COORD MODES
9-12	AX1-4	Auxiliary MSD CKT's 1-4
13	SYS	Call for system--see COORD
14	MX2	Call to Max II (both rings)
15/16	IM1/2	Inhibit Max ring 1/2
17/18	CN1/2	Call to Non Act I/II
19	MIN	Min Recall all phases
20-27	VC1-8	Vehicle call 1-8
28-35	PC1-8	Ped call 1-8
36-43	VO1-8	Vehicle omit 1-8
44-51	PO1-8	Ped omit 1-8
52	CSV	Conditional service (enable)
53	SGO	Simultaneous Gap-Out (inhibit)
54	INT	Interconnect inhibit
55	SYN	Sync Inhibit (offset outputs)
56	WRM	Walk Rest Modifier (enable)
57	DLE	Dual Entry (enable)
58/59	RR1/2	Red Rest Mode ring 1/2 (enable)
60/61	OR1/2	Omit Red Clearance ring 1/2
62/63	PR1/2	Ped Recycle ring 1/2 (enable)
64	DLI	Detector Low threshold Inhibit
65	DPI	Det (continuous) Presence Inhibit
66-71	PE1-6	Pre-empt call 1-6
72-79	MP1-8	Max Plans 1-8
80-87	SP1-8	Service Plans 1-8

(continued)

CLOCK CKT DESCRIPTION (continued)

CKT	ABBREV.	FUNCTION
88-91	LG1,3,5,7	Lag phases 1, 3, 5, 7 (alt.seq.)
92-99	VD1-8	Inhibit Volume Density phase 1-8
100	EXP	Exclusive ped (enable)
101-108	I17-24	Inhibit detectors 17-24
109	ASC	Enable Adaptive Split Control
110-113	OLA,B,C,D	TOD Inhibit overlaps A, B, C, D
114/115	AT1/2	Enable schd A to call phone 1, 2
116/117	BT1/2	Enable schd B to call phone 1, 2
118/119	CT1/2	Enable schd C to call phone 1, 2
120-135	ID1-16	Inhibit detectors 1-16
136	EAV	Enable alternate vol. sample per.
137/8	VT1/2	Enable vol. data to call ph # 1, 2
139	EVL	Enable volume logging
140	EAM	Enable alt. MOE sample period
141	EML	Enable MOE logging
142	ICP	Inhibit Conditional Ped
143	IDD	Inhibit Detector Delay
144	CTF	Call to Free
145	DEP	Dual Enhanced Ped
146	I5H	Inhibit 5 section head control
147	CTC	Call to time clock mode
148	IYR	Increase Yellow & Red
149	DIM	Enable Dimming
150	W10	Call to week program 10

Time Clock CKT notes (review before using CKTS):

1. Ckt's. 64, 65 are related to detector failure monitoring and would be applied at certain times of day to prevent unwanted detector failures. Low threshold inhibit disables no activity and low threshold monitors, while continuous presence inhibit disables constant call. Typically, DLI would be applied in the "wee" hours of the morning and DPI would be applied at rush hour (particularly if long loops that might be continuously occupied are used).

2. Ckt's 66-71, pre-empt calls, have associated inputs on MSD which are the normal means of applying pre-empt calls. However, these ckt's are useful for keyboard testing pre-empt calls (manually on), or for time of day initiated pre-empt sequences like soft flash (see pre-emption).

3. Ckt's 72-79, 80-87 are used to select max and service plans 1-8. However, these plans can also be selected by combination of cycle and split which will override time clock selection when both are active (see coordination).

4. Ckt's 88-91, lag phases 1, 3, 5, 7, are only operational if the sequence is programmed "Lead/Lag" and the corresponding pair (1&2, 3&4, 5&6, 7&8) are programmed "Auto"--thus allowing automatic reversal.

5. Ckt's 92-99 inhibit volume density operation on the corresponding phase, including S/A, TBR, TTR, and Min Gap.

6. Ckt 100 is exclusive ped. When enabled, peds 2, 4, 6, 8 become simultaneous and exclusive--they all display walk at the same time, with no greens, following the clearance of phase 2 (and 6). When the exclusive mode is enabled, the timing of the walk and ped clear are obtained from *phase 1* walk and ped clear. Each ped times normally with its own timing when ckt 100 is inactive. For full time exclusive ped, simply program ckt 100 on (manual).

7. Ckt's 110-113, TOD overlap inhibits, force the indicated overlap to red until de-activation of the circuit. When necessary, clearances are obtained from *overlap delay* yellow and red, while min green comes from pre-empt # 1 min grn entry. Thus, **you must** load pre-empt # 1 **ENTRY MGR** plus the corresponding overlap delay yellow and red for any clock inhibited overlap (delay = 0 = no delay). The inhibit overlap circuits do not override overlap operation during pre-emption. If the pre-empt sequence allows the overlap, it will be allowed even if clock inhibited.

8. Ckt's 114-119 are related to the call-in of reports when the LMD is operating in the direct dial-up mode. Each of a number of functions can be assigned to a schedule A, B, C, or Request Only (see reports). Each of the schedules A, B, and C can then call into telephone 1 or 2 according to the activity of the associated circuits as follows:

	Call	Circuits					
Function	**Phone**	**114**	**115**	**116**	**117**	**118**	**119**
Sched A	None	OFF	OFF	*	*	*	*
Sched A	Phone 1	ON	OFF	*	*	*	*
Sched A	Phone 2	OFF	ON	*	*	*	*
Sched A	Both	ON	ON	*	*	*	*
						*= don't care	
Sched B	None	*	*	OFF	OFF	*	*
Sched B	Phone 1	*	*	ON	OFF	*	*
Sched B	Phone 2	*	*	OFF	ON	*	*
Sched B	Both	*	*	ON	ON	*	*
Sched C	None	*	*	*	*	OFF	OFF
Sched C	Phone 1	*	*	*	*	ON	OFF
Sched C	Phone 2	*	*	*	*	OFF	ON
Sched C	Both	*	*	*	*	ON	ON

With the use of these clock circuits, the rate at which the LMD calls in for certain functions call be pre-determined. For example, high priority functions could be assigned (see reports) to schedule A, and A phone ckt's could be programmed ON all or much of the time. Similarly, schedule B could be set up to call once per day, while C calls in once a week. Also, the ckts can be used to call one phone, say in the day, and another at night, etc.

9. Ckt's 120-135 inhibits detectors 1-16. This feature can be used to effectively disable or switch detectors (by disabling one then the other at the appropriate times).

10. Ckt 's 136-139 are used for local volume logging. Ckt 136 enables the alternate sampling period. 137 and 138 allow volume data to be called in to T1 and T2 in the direct dial mode. Ckt 139 enables volume logging and is only activated during times of day it is desired to collect data.

11. Ckt 146 inhibits 5 section head yellow blanking and phase restrictions even if programmed for that mode.

12. Ckt 147, Call to time clock, is used to force the unit into time clock selection of Cycle, Split, offset, Flash and System *regardless* of the normal programmed mode of selection. A typical use would be to force the LMD into the time clock mode during peak periods--even though it is programmed for the traffic responsive mode.

13. CKT 148, Increase yellow and red, causes all yellows and reds to time a value greater than normal by the percentage amount specified under controller options.

Note: We do not recommend using I Y & R for routine circumstances like night versus day--as drivers may become accustomed to one set of timings versus another. I Y & R is intended to be activated under special circumstances such as inclement weather. This can be accomplished by activating CKT 148 only during special day programs assigned to week program 10. See note 14 below.

14. Ckt 150, Call to week program 10, can also be activated by a special input on MSD pin 11. This function forces the LMD clock to week program 10, overriding the normal week program. The LMD returns to the normal week program when the ckt or input is de-activated--as events are updated on transitions. Typical use would be for unanticipated circumstances. For example, the LMD could be set up with special "bad weather" day programs assigned to week program 10, remotely activated (by input or downloading ckt 150 ON) as needed.

WEEK PROGRAMS

PG DWN or PRIOR MENU...Selection 6...WEEK PROG....

```
          --WEEK PROGRAMS--
WK P |DAY OF WEEK   S  M  T  W  T  F  S
  1  |DAY PROGRAM   2  1  1  1  1  1  2
          --PGDN TO CONTINUE--
```

PG DWN, etc...up to 10 week programs.

Specify the day program to be assigned to each day of the week for that week program. The week program above has been assigned day program # 1 on weekdays and day program # 2 on Saturday and Sunday.

YEAR PROGRAM

PRIOR MENU...Selection 7...YEAR PROGRAM

```
  --YEAR PROGRAM BY CALENDAR DATE--
FROM: MOY DOM   TO: MOY DOY   WEEK PROG
        1/01          12/31         1
         --PGDN TO CONTINUE--
```

Specify the "FROM" and "TO" date for each week program to assigned. Start with 1/01, continuing until the "TO" date is 12/31. The default year program shown above requires only one screen because it covers the entire year.

Note that week programs *start on Sundays*. However, the LMD counts the year in weeks, starting on Jan 1. Thus, when specifying multiple week programs in one year, try to choose the same day of the week that Jan 1 occurred on as "from" and "to" days. Also, each "to" date (if not 12/31) should be the *week before* the next "from" date. If not, the controller will automatically make the described adjustments. However, if you wish to see exactly what you loaded, then follow this format.

DAY PROGRAMS

PRIOR MENU...Selection 8..DAY PROGRAMS

```
          --DAY PROGRAMS--
DAYPROG| EVENT TIME | CSO-OR-CKT ON/OFF
   1   |  06:00:00  |  111
--PGDN OR PGUP TO READ--     EVENT NO.1
```

PG DWN.....to next event

```
          --DAY PROGRAMS--
DAYPROG| EVENT TIME | CSO-OR-CKT ON/OFF
   1   |  06:00:00  |        13   ON
--PGDN OR PGUP TO READ--     EVENT NO.2
```

PG DWN ETC....through the remaining events.

PROGRAMMING DAY PROGRAMS

1. There are 2 distinct types of events, and both use the same type screen, **but only one type** can be specified per event. Up to 200 total events can be programmed.

   Coordination CSO events. These specify the cycle, split and offset to be implemented at the indicated time. The first day program screen shown is an example of a coordination plan event; cycle 1, split 1, offset 1.

   Circuit events. These are for circuits 8-150, the second day program screen shown is an example of a circuit event screen, where:

   CKT 8 = call for flash

   CKT'S 9-12 = AUX circuits 1-4

   CKT 13 = call for system.

   CKT 14-150 = see time clock circuit list.

   Note: All clock circuits and CSO selections are reset to default values at midnight (CSO = 110, ckt's= Off)

2. Event Counter. The lower right corner of the display lists the events, numbered in chronological order, where the first event of the first programmed day program is event # 1. As you load events, the LMD will automatically assign an event number, inserting it into the order of all other events previously loaded. Any new event will be assigned a number in its correct order, and all higher numbered events will be incremented by 1.

3. To read previously loaded events,

   a. You can simply start at event # 1 and page down through the events. The display will initialize to event # 1 (usually the first event of day program # 1), and will increment through events in order by paging down.

   or

   b. You can specify the day program by entering 1-15 and hitting ENTER. You can then specify the event time by entering 6 digits and hitting ENTER. The display will increment to the next event occurring after that time.

   Note that you can read events by manipulating the day and hour using the *ENTER* key, then paging down for further events after that point. *Data is not changed* until the CSO for CKT fields are manipulated.

4. To load events:

a. First, specify the day program number 1-15, then use the arrow key to move to the time field.

b. Then, set the event time by keying 6 digits and using the arrow key to move to the event field.

c. Next, when you get to the event field, you have a *choice* of a coordination CSO event or a CKT event.

To load a coordination CSO event, move the arrow key to the left side of the event field and enter a CSO selection 111-845. As soon as you arrow right, the event will be recorded and the event counter will update*.

To load a circuit (8-150), move the curser to the right side of the event field under CKT and key a value 8-150. Then, arrow right (the cursor will be under ON/OFF) and key in ON or OFF and arrow right or ENTER--the event is stored and the event counter will update*.

***The term "update"** is used here because the LMD will record all events in chronological order, starting with the *first event of day 1*. Thus, when you load a new event, the event counter will reflect the new event's position relative to all other events.

5. To continue to load events, do not page down. Simply re-specify the day (if different), time (if different), and CSO or CKT ON/OFF in the same fashion, on the same screen. The old event has already been recorded. Note that you cannot "write over" an event once loaded. An event can only be removed by using the delete procedure.

6. To delete an event, bring up the subject event screen by either of the read methods in note 3.

To delete a CSO event, arrow the cursor right until it points to the CSO to be deleted, then enter 0 (delete). The CSO event will be deleted. **To delete a CKT event,** also arrow the cursor right until it points to the CSO position (even though there is nothing there), then enter 0 (delete). The CKT event will be deleted.

To delete multiple events, the easiest way is to position the cursor on the CSO position of the first event, then hold one finger above 0 (delete) and another above ENTER. Push 0 then ENTER. As each event is deleted, it will be replaced by the next chronological event. Push 0 again then ENTER to delete that event. Continue this process as desired.

Note: You must use the delete procedure to delete events because you cannot replace an event by loading a new event, even if it is for the same day program at the same time of day--old events are stored until deleted or a "Clear Time Clock" is executed from the Utilities Menu.

7. If the time clock has never been cleared, the screen will prompt you to do so when you attempt to enter the first event. Go to the utilities menu to clear the clock data.

TIME /DATE SET ROUTINES

These routines allow the Time, Date, and Year to be set.

PRIOR MENU...Selection 9...TIME SET

```
        --TIME OF DAY SET--
CURRENT TOD   | KEY IN NEW VALUES THEN
  --:--:--    | ENTER TO SET NEW TIME
        --PG DN TO CONTINUE--
```

Enter time as 6 digits based on 24 hour clock (4 P.M. = 16:00:00). Enter a value slightly ahead of the real time then press ENTER at the *precise moment* that the real time equals the time entered. The value disappears if accepted.

PG DWN

```
              --DATE SET--
YEAR    DATE  | KEY IN NEW VALUES THEN
         /    | ENTER TO SET NEW DATE
          --END OF SECTION--
```

Key in the year as 4 digits, arrow right (the year disappears) then load the date as month/day of month. **Always load the year first**, then load the date (Update after setting).

SECTION VII

PRE-EMPTION AND TRANSIT PRIORITY PROGRAM/READ MODE

GENERAL

The LMD9200 provides a low and a high priority pre-emption sequence for each of 6 pre-empt inputs on MSD. There are also 6 pre-empt outputs which can be controlled by the pre-emption sequences. To program pre-emption:

PROGRAM READ, SELECTION 5, PRE-EMPTION

```
        --PRE-EMPTION DATA--
1-6. PROG SEQS 1-6     8. HI PE SET-UP
7.SPEC INT VALS .1-.9  9. LOW PRIOR PE
```

PROGRAMMING SEQUENCES....Selections 1-6...

Each sequence consists of up to 15 steps. The first step of the sequence determines the entry phase(s) to which the LMD will initially pre-empt to upon activation of the input. The first step must be a phase, a compatible dual ring phase pair such as 26, 37, etc., or All Red (code “90").

For example, selecting sequence #1...

```
SEQ1|PHS-SPECL|TIME|HOI  |PE-OUTS|90=RED
  1 |16       | 25 | ON  |   1   |99=RET
  2 |99       | 0  |OFF  |       |.1-.9=
  3 |         | 0  |OFF  |       |SPEC'L
```

PG DWN to access instruction steps 4-6, 7-9, etc.

INSTRUCTION SET

After the first step, other phases can be specified, a “special Interval or a code, where:

1-8 = Phases 1-8 allowed
.1-.9 = Special intervals
89 = Hold on input w/gap (see page 7-8)
90 = Go to All Red
91 = CVM OFF (flash)
92 = CVM ON
93 = Enable Peds during pre-empt
94 = Inhibit peds during pre-empt
95 = Go to Priority Return phases (see pg. 7-9)
96 = Enable coordination
97 = Strict permissives enabled
98 = Exit pre-empt, no calls
99 = Exit pre-empt, ped calls all phases

T IME = 0-9.9 or 127 secs, timing of step

Acts as min time if HOI = ON
Acts as step time if HOI = OFF

The timer begins as soon as the phases specified by the step are achieved. Use a minimum of .1 second timing for all instructions except 91-99 which can all use 0. The times below are special cases;

If Time =.0 for the first step, barrier phases in different rings can clear independently (e.g. 2 & 6). Otherwise they wait until both can clear, then clear together only. Repeat the second step with same phases as the first using the “real” hold time when using .0 for the first step.

If Time = 0 for 95 priority return instruction, it actually times .2 secs

Time = gap time if 89 code used—see page 7-8

HOI = “Hold on Input” (On/Off). If On, the unit holds the step after the timer times out until the input goes away. If Off, it exits the step after timing out. When holding, the step phases and conditions are maintained.

OUTPUTS = Pre-empt outputs activated during that step:

1-6 = PE 1-6 out
7 = Flash suffix (e.g. 17 = flash PE output 1)

Output note: If Time = 0 for the first step, any PE outputs specified in the first step come on with the input, even before pre-empt entry is initially achieved. The pre-empt step entry phases would then be repeated in step 2 with the real entry phase hold time programmed.

General Operation

When an instruction step finishes timing, it proceeds to the next step. If the current phases are not specified in the next step or are not compatible with phases in that step, they will immediately be forced off. Each step can consist of a phase, a compatible phase pair, or any comb-ination of non compatible phases 1-8. When non comp-atible phases are specified, the unit will cycle between them. One call Is placed on all step phases upon entry Into the instruction. After that they are “on their own”.

When one a 91-97 type instruction is executed, the phases (or All Red) specified from the last previous phase instruction will remain in effect until a new instruction including phases (or All Red) is executed.

Peds are normally inhibited into and during pre-emption. Use code 93 to re-enable peds from that point forward—to the end of pre-empt or until a 94 code.

The 96 and 97 codes pertain to coordination. Code 96 en-ables coordination during preemption, typically used during long pre-empts. Code 97 is usually executed just prior to exit (the step before 98 or 99). This invokes strict permissives upon exit from pre-emption so that only phases allowed by the coordinator’s permissives will be served. This helps to maintain coord after pre-empt.

SPECIAL INTERVALS (Defining)...Selection 7...

Special intervals are called for in the pre-empt sequence table—they are **defined** in this section. Special intervals are used when normal pre-empt steps by themselves cannot completely do the Job. Normal pre-empt steps allow the **LMD** to go to a phase, cycle phases, go to all red, etc. Special Intervals allow configuration as desired.

```
 --SPEC INT .1 PH/0L-- 10=DK 1=G 2=GW
1 2 3 4 5 6 7 8 A B C D13=FDW 4=Y 5=R
5 5 5 5 5 5 5 5 5 5 5 516=FYWIG 7=FYWAG
DECIMAL PT= FAST FL GRN18=FRWIG 9=FRWIG
```

The special interval above is configured for ALL Red.

SPECIAL INTERVAL CODES:

0 = DARK (NO OUTPU1)
. = FAST FLASH GREEN (CANADIAN LTURNS)
1 = GREEN/DON'T WALK
2 = GREEN/WALK
3 = GREEN/FLASHING DON'T WALK
4 = YELLOW
5 = RED
6 = FLASH YELLOWWG (1 HZ)
7 = FLASH YELLOW WAG (1 HZ, 180° out of phase)
8 = FLASH RED WG (1 HZ)
9 = FLASH RED WAG (1HZ,180° out of phase)

Note that the **'WIG vs. 'WAG"** simply denotes that the flash cycles are 180 degrees out of phase with each other.

RULES FOR SPECIAL INTERVALS

1. The controller must enter special intervals from all red. That is , the controller must execute a "90" code prior to execution of special interval.

2.The controller must exit special intervals from all red.Once any special interval has begun, the sequence must continue executing special intervals until the last special interval is all red (all 5's). In other words, once a special interval is used, the sequence steps must continue with special intervals, configured in such a way as to drive the controller back to all red (special interval with all 5's).

The above rules are necessary because the "special intervals" provide a great deal of power to the user, i.e. the ability to take over the controller phase/ overlap outputs. Normal controller operation must be suspended during this period. To accomplish this, the controller essentially "waits in all red" until the manipulation of the outputs is done. Thus, you must enter special intervals from all red (code 90), then return to all red (all 5's), using special intervals before returning to normal controller operation. If this is not done, the sequence will not be executed.

PRE-EMPT SET-UP...Selection 8...

The pre-empt set-up menu appears as follows:

```
          --PE SET-UP--
1.MEM/DEL/RESVC 4.PRIORITIES 7.PRIOR RET
2.0/L INHIBITS  5.HOLD ONLY
3.ENTRY TIMES   6.DELAY OPTION
```

MEMORY/DELAY/RESERVICE...Section 1...

INPUT	1	2	3	4	5	6	
MEMORY	OFF	OFF	OFF	OFF	OFF	OFF	10N/OFF
DELAY PE	0	0	0	0	0	0	10-255S
MIN RESV	0	0	0	0	0	0	10-99M

PRE-EMPT INPUT MEMORY ON/OFF. Determines the pre-empt Input memory status. When on, the pre-empt call is locked in memory until preempt completion.

When off, the call is not locked, but in most cases, since pre-empt is immediate, preemption will still follow through until completion—i.e. once pre-empt is started it will complete whether memory is on or off. Memory off only has a significant effect if the input has a delay before preempt, In which case if the call goes away during the delay period, preemption will not be served.

DELAY PE Starts with activation of the input, the pre-empt sequence does not take effect until timer times out. Will not serve pre-empt if memory **is off** and input goes away before timer times out. **Also, see** the "Delay Option" which allows peds and non-pre-empt phases to be omitted during the "Last X secs" of the delay period when desired. This time is user specified for each input. This feature basically allows the phase active during that last portion of the delay before pre-emption to time normally, but if it gaps or max's out, the controller will proceed directly to the pre-empt phases (omits applied).

MIN RE-SERVICE. Sets minimum time period for each input, in minutes, between successive preempt sequences. Usually used with low priority sequences to prohibit excessive preempting. Set to zero for high priority sequences such as fire and train, indicating that there is no restrictions on successive pre-emptions. The timer starts after a pre-empt sequence, upon the return to normal operation.

PRE-EMPT OVERLAP INHIBITS...Selection 2

```
     --PE O/L INHIBITS--        |0=NORMAL
PE-1 PE-2 PE-3 PE-4 PE-5 PE-6  |1=INHIB.
0000 0000 0000 0000 0000 0000  |----ABCD
     --END OF SECTION--
```

Overlap Inhibits determine the status of each of the 4 overlaps during each of the 6 pre-empt sequences. The 4 digits represent overlaps ABCD respectively.

If a "1" is associated with the overlap, it will be cleared upon entry into the pre-empt sequence and will remain red throughout. If the overlap must be cleared in a circumstance that it normally would not clear, then it will use the special pre-empt overlap times–see "Entry Timing".

If a "0" is programmed the overlap will operate as it normally would throughout pre-emption.

ENTRY TIMINGS....Selection 3...

```
    --PE ENTRY TIMINGS INPUT #1--
MGR WLK PCL OLY OLR FDW/Y | USED FOR PE
 5   1   7   4   2  OFF  | ENTRY ONLY
  (0-9.9 OR 127)  (OFF/ON)
```

PG DWN, etc....For inputs 2-6.

PRE-EMPT ENTRY TIMINGS essentially determine the responsiveness of the associated input upon entry into pre-emption. These timings override the normal controller settings, *except* for the **value 0,** which is a special code used for MGR, WLK or PCL indicating the *normal programmed phase* values will be used. Any other value from .1-99 will override normal controller settings upon entry into pre-emption. **When FDW/Y= ON** the controller will flash the Don't Walk thru Yellow on entry into pre-emption (only). Used when there is little time to pre-empt (RR).

These settings are on a per pre-empt input basis so that the responsiveness of each input can be adjusted accordingly. For example, high priority pre-empts such as railroad or emergency vehicle sequences would use low values so that the response is rapid. Low priority pre-empts, such as bus or soft flash, would use higher values since there is less urgency to get to pre-emption.

The overlap timings provide clearance times for clearing overlaps upon entry into pre-emption–see overlap inhibits.

PRIORITIES...Selection 4....

```
     --PRIORITY OF PE SEQUENCES--
INPUT 1 2 3 4 5  6|PRIOR 1-6, USE SAME
PRIOR 6 6 6 6 6  6|NO. FOR ALL W/SAME.
FL/OV 0 0 0 0 0  0|FL/OVER:1=OVERRIDE
```

PRIORITY. This programming determines the relative priority of each of the sequences, 1 being highest, 6 being lowest. A higher priority sequence will override a lower priority sequence--even if already in the lower priority sequence. In such a case, the LMD will leave the active sequence and serve the higher priority pre-empt, clearing phases as necessary. Pre-empts of equal priority are on a first come, first serve basis. A pre-empt sequence will not be overridden by a pre-empt of equal or lower priority.

Note that if special intervals are active and a higher priority sequence becomes active, the LMD will advance to and time the next special interval, then to the next, and so on until the controller gets back to a non-special interval--from which it can proceed in normal pre-empt fashion to the higher priority sequence. In cases where the LMD must override a pre-empt during special intervals, it will **time no more than 7 seconds** in any one special interval.

FL/OV (Remote Flash Override). This setting determines if the pre-empt sequence will override Remote Flash (this is planned "Hard" Flash, where the flash transfer relays are purposely dropped). Recall that Remote Flash is the CVM initiated flash due to time clock command, MSA Test A, or the MSD Interconnect flash input.

When programmed "1" and the pre-empt input is activated during remote flash, the LMD will exit flash into the **flash exit** phase & interval. Pre-emption starts there.

When programmed "0", the LMD will not exit remote flash to serve the pre-empt sequence. In addition, if the input is in the *memory off* mode, the LMD will not exit flash, *even when scheduled to*, until the pre-empt input goes away. Prevents exiting flash in the middle of PE.

HOLD ONLY...Selection 5...

INPUT	1	2	3	4	5	6	1ON=HOLD
ON/OFF	OFF	OFF	OFF	OFF	OFF	OFF	1ONLY. NO
PHASES							1PE SEQ.
TIME	0	0	0	0	0	0	1REQUIRED

HOLD ONLY PRE-EMPT allows a special type of "soft" pre-emption" in which a phase (or phase pair) can be held for a specific period of time—but only when the associated phase is green. It will not pre-empt out of other phases or otherwise disrupt their timing. When designated as "Hold Only", (ON) there Is no pre-empt sequence, only the ability to hold a phase that Is already green. When 'Hold Only" is off, the pre-emption is a sequence type preemptor and a sequence must be created. The time value begins with activation of the input. The phases will be held until the timer times out or until the input goes away—whichever happens last. "Hold Only" would typically be used for bus pre-emption, or for release of congested queues (used with a set back loop with a delay).

DELAY OPTION...Selection 6...

--OMIT DURING DELAY BEFORE PE OPTION--						
DELAY B4 PE #	1	2	3	4	5	6
PED OMIT LAST X	0	0	0	0	0	0
VEH OMIT LAST X	0	0	0	0	0	0

The delay option relates to the "last x" seconds of the delay before preemption period.

During the PED OMIT LAST X period, no pedestrian movements can start if not already timing. During the VEH OMIT LAST X period, only pre-empt phases can start if not already timing. Entry phases are the phases Included In the first step of the sequence. The Delay option can be used to "prep" the intersection for the forthcoming pre-empt by not allowing late service to peds or non pre-empt phases just before the delay times out. The feature only prevents the start-up of phases and peds (by omit), it does not force termination of already timing movements until hard pre-empt occurs after the delay times out.

LOW PRIORITY PRE-EMPTION (LPPE)

LPPE provides a means of using the standard 6 pre-empt inputs for additional low priority pre-empts. A low priority input signal is defined as a 6.25 HZ nominal squarewave (3M Opticom). Each pre-empt input can thus have both a high and a low priority pre-empt, since the steady high priority signal would always override the pulsed signal Any high priority PE thus overrides and exits if necessary, any low PE. Low priority PE's are on a 1st come, 1st serve basis amongst themselves.

SELECTION 9 FROM PRE-EMPT MENU....

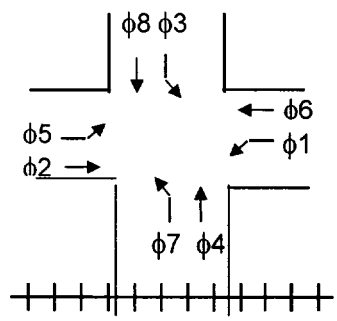
--LOW PRIORITY PRE-EMPT INPUT DATA--								
	MEM	MGR	WLK	PCL	OLY	OLR	DEL	OMT	RESV
LP1	OFF	5	1	7	4	2	0	0	0
LP2	OFF	5	1	7	4	2	0	0	0

Sequence programming for LPPE begins at step 10 of the PE sequence, i.e. program the normal sequence with steps 1-9, low priority with 10-15. The sequence programming is *otherwise the same* as for standard preempts.

The set-up data operates the same as for standard preempts where: MEM = memory on/off, MGR = Preempt min green, WLK preempt entry min walk, PCL = pre-empt entry min ped clearance, OLY & OLR= preempt overlap yellow and red, OMT = "omit last X' time, and RESV = min re-service time (in minutes).

EXAMPLE PRE-EMPT SEQUENCES

The following example set applies the preempt capabilities and will be defined in terms of general goals and how those are applied to each of the pre-empt programming segments. Consider the 8 phase intersection below:



From this configuration, assume the following pre-empt sequences are desired:

SEQ	DESCRIPTION	PRIORITY
1	Fire. Go to phases 1 and 6 for 25 seconds. Hold till input goes away. Turn on PE1	2nd highest
2	Fire. Go to phases 2 and 5 for 25 seconds. Hold till input goes away. Turn on PE2	2nd highest

SEQ	DESCRIPTION	PRIORITY
3	Fire. Go to phases 3 and 8 for 25 seconds. Hold till input goes away. Turn on PE 3	2nd highest
4	Fire. Go to phases 4 and 7 for 25 seconds. Hold till input goes away. Turn on PE 4	2nd highest
5	**Railroad.** Go to phases 4 AND 7 track clearance for 20 secs., then cycle normally phases 2,3, 4,5,6,7 only until the input goes away (1,8 cross the track).	Highest
6	**Soft flash**–load switch flashes signals. Enter into soft flash after serving 4 & 8 and clearing to all red. Flash 2 & 6 yellow, flash 1,3,4,5,7,8 red until input goes away. Exit flash into 2 and 6 green for 20 seconds.	Lowest

Notes:

1. Sequences 1-4 are of *equal* priority with respect to each other (1st come, 1st serve), but will override sequence 6. Sequence 5 is the *highest* priority and will override all others.

2. All sequences except 6 will override controller remote flash, which is often called "hard planned flash" because the CVM output is used to cause the monitor to drop the flash transfer relays. Do not confuse hard remote planned flash with conflict monitor flash due to unplanned failures. No pre-empt sequence will override flash due to unplanned failure (conflict, red failure, clearance failure, etc.).

PROGRAMMING THE EXAMPLE PRE-EMPT SCREENS

SEQUENCE PROGRAMMING

From the Pre-empt menu, selections 1-6....

FIRE SEQUENCES. Sequences 1-4 are the fire run sequences and only require 2 steps each. The first step simply specifies the phases to go to, the time, and the "Hold on Input" status. The "Hold On Input" feature is on during the first step of each of the fire run sequences, indicating that the LMD will remain in those phases until the input goes away.

The time begins with the phases, and provides the minimum service time. The LMD holds beyond the timer value only if the input is still active.

NOTE; For phases and all red (code 90), at least .1 second timing must be programmed.

Also note that the appropriate pre-empt output is turned on in each case.

Code 99 returns to normal operation, placing calls on all phases (code 98 returns without placing any calls).

SEQUENCE # 1....Fire run, phases 1&6

SEQ	PHS-SPECL	TIME	HOI	PE-OUTS	90=RED
1	16	25	ON	1	99=RET
2	99	0	OFF		.1-.9=
3		0	OFF		SPEC'L

PRIOR MENU...SEQUENCE # 2...Fire run, phases 2&5

SEQ	PHS-SPECL	TIME	HOI	PE-OUTS	90=RED
1	25	25	ON	2	99=RET
2	99	0	OFF		.1-.9=
3		0	OFF		SPEC'L

PRIOR MENU...SEQUENCE # 3...Fire run, phases 3&8

SEQ	PHS-SPECL	TIME	HOI	PE-OUTS	90=RED
1	38	25	ON	3	99=RET
2	99	0	OFF		.1-.9=
3		0	OFF		SPEC'L

PRIOR MENU...SEQUENCE # 4...Fire run, phases 4&7

SEQ	PHS-SPECL	TIME	HOI	PE-OUTS	90=RED
1	47	25	ON	4	99=RET
2	99	0	OFF		.1-.9=
3		0	OFF		SPEC'L

RAILROAD SEQUENCE

Sequence 5 is the railroad pre-emption sequence. Phases 4 and 7 are the track clearance phases, followed by phases 2, 3, 4, 5, 6, and 7. The controller will cycle normally between these phases until the input goes away (phases 1 and 8 are omitted because they would cross the track). The time duration of step 2 or the active input duration–whichever is longer–specifies the duration of the period in which omits are applied to phases 1 and 8.

PRIOR MENU...SEQUENCE # 5...Railroad, 4&7 track clear

SEQ1	PHS-SPECL	TIME	HOI	PE-OUTS	90=RED
1	47	20	OFF	5	99=RET
2	234567	10	ON	5	.1-.9=
3	99	0	OFF		SPEC'L

Notice that the output remains on in both steps 1 and 2. Also note that the first step specifies a compatible phase pair, thus the controller will hold in these phases. Step 2, however, allows several non-compatible phases, thus the controller will cycle between them.

SOFT FLASH SEQUENCE..selection 6

Sequence 6 is the "Soft Flash" sequence. This sequence requires a bit more programming because of the use of "special Intervals". The special intervals must be defined as well as specified in the sequence.

Step 1 in this sequence is to cycle to phases 4 and 8.

Step 2 takes the controller to all red (code 90).

Steps 3-6 are all special intervals (see special interval programming).

Step 7, after the "All Red" special interval, is an All Red "90 code" --but with only .1 second timing. The purpose for this step is to provide a point of exit in case a higher priority pre-empt takes the LMD out of soft flash. Recall that when a higher priority pre-empt overrides special intervals, the LMD keeps timing thru the special intervals in order until a "normal" interval is timed (90 = All Red is considered "normal"). Without the "90 code" the next "normal" interval would be phases 3 and 7 (see the next paragraph) and the LMD would be committed to timing the minimum time of 3 and 7, plus yellow & red. With the "90 code" inserted, the overriding entry phase can be immediately serviced after step 7. The value of .1 is used because the All Red period has already been timed, this is just a point of exit in case of override.

Step 8. At this point, It would be tempting to exit preemption, since special intervals are over and all red has been timed. However, step 8 is used to take the controller to 3 & 7. This is basically to insure that the controller **will go** to 3 and 7. Since 2 and 6 green is timed by special intervals, 3 & 7 *should* be served next. The problem in this case is that the controller "wants to go" to 1 and 5. This is because it was last in *normal* operation when it was clearing from 4 & 8--before the special intervals were timed. Thus, 1 & 5 would have been the next phases *normally* served. But this not what is now desired, so the "37" instruction is inserted. Note that the time duration of the "37" instruction is only 5 seconds. It could have been .1 or 1 seconds (not zero) because the idea is to simply get it to 3 and 7, then return to normal.

Step 9 returns to normal operation with calls on all phases.

PRIOR MENU...SEQUENCE # 6...Soft flash

SEQ6	PHS-SPECL	TIME	HOI	PE-OUTS	90=RED
1	48	15	OFF		99=RET
2	90	2	OFF		.1-.9=
3	.1	10	ON	6	SPEC'L

PG DWN...

SEQ6	PHS-SPECL	TIME	HOI	PE-OUTS	90=RED
4	.2	20	OFF		99=RET
5	.3	4	OFF		.1-.9=
6	.4	2	OFF		SPEC'L

PG DWN...

SEQ6	PHS-SPECL	TIME	HOI	PE-OUTS	90=RED
7	90	.1	OFF		99=RET
8	37	5	OFF		.1-.9=
9	99	0	OFF		SPEC'L

SPECIAL INTERVAL PROGRAMMING

In the example, the first special interval is the soft flash interval. Note that, in this case, all indications either flash or are red (the overlaps). The flash rate of 1 HZ (50% duty cycle) should be within the limits of the 800 millisecond recognition time of the conflict monitor.

Note, however, that If any of the phases/overlaps should be programmed to go dark in your application, you will need to use a pre-empt output, activated during the soft flash interval, to drive a + 24VDC relay which will inhibit the Red Monitor. Otherwise "Red Failure" would occur.

EXAMPLE SPECIAL INTERVALS

To program the special intervals:

PRIOR MENU...Selection 7....SPEC INTERVALS .1-.9

The 1st special interval is the "Soft Flash" interval. Note how the "WGS" and "WAGS" have been allocated.

```
-- SPEC INT .1 PH/OL--  |0=DK 1=G 2=GW
1 2 3 4 5 6 7 8 A B C D |3=FDW 4=Y 5=R
9 6 8 9 8 7 9 8 5 5 5 5 |6=FYWIG 7=FYWAG
DECIMAL PT= FAST FL GRN |8=FRWIG 9=FRWAG
```

PG DWN...The 2nd is phase 2 and 6 green (flash exit).

```
-- SPEC INT .2 PH/OL--  |0=DK 1=G 2=GW
1 2 3 4 5 6 7 8 A B C D |3=FDW 4=Y 5=R
5 1 5 5 5 1 5 5 5 5 5 5 |6=FYWIG 7=FYWAG
DECIMAL PT= FAST FL GRN |8=FRWIG 9=FRWAG
```

PG DWN...The 3rd is phase 2 & 6 yellow

```
-- SPEC INT .3 PH/OL--  |0=DK 1=G 2=GW
1 2 3 4 5 6 7 8 A B C D |3=FDW 4=Y 5=R
5 4 5 5 5 4 5 5 5 5 5 5 |6=FYWIG 7=FYWAG
DECIMAL PT= FAST FL GRN |8=FRWIG 9=FRWAG
```

PG DWN...The 4th and last special interval is All Red

```
-- SPEC INT .4 PH/OL--  |0=DK 1=G 2=GW
1 2 3 4 5 6 7 8 A B C D |3=FDW 4=Y 5=R
5 5 5 5 5 5 5 5 5 5 5 5 |6=FYWIG 7=FYWAG
DECIMAL PT= FAST FL GRN |8=FRWIG 9=FRWAG
```

Note that this last interval is all red (all 5's) and is the required interval before exiting the special intervals.

Also note that although it would appear possible to simply exit the special flash interval into 2 and 6 green using a standard "26" type instruction and not a "special" interval, it is not allowed--**special intervals must be continued** until the controller is brought back to All Red. Thus, time 2&6 green, yellow and red using special intervals, then exit back to a "normal" interval.

PRE-EMPT SET UP FOR THE EXAMPLE

PREV MENU...SELECTION 8..**PE SET-UP...**

```
          --PE SET-UP--
1.MEMORY/DELAY/RESERVICE  4.PRIORITIES
2.OVERLAP INHIBITS        5.HOLD ONLY
3.ENTRY TIMINGS           6.DELAY OPTION
```

MEMORY/DELAY/RESERVICE.....Selection 1..

```
INPUT     1   2   3   4   5   6
MEMORY    ON  ON  ON  ON  ON  ON  |ON/OFF
DELAY PE  0   0   0   0   0   0   |0-255S
MIN RESV  0   0   0   0   0   0   |0-99M
```

All sequences have memory on, there is no delay before pre-empt and there is no minimum re-service.

PRE-EMPT OVERLAP INHIBITS...(PRIOR MENU) Selection 2....

```
     --PE O/L INHIBITS--        |0=NORMAL
 PE-1 PE-2 PE-3 PE-4 PE-5 PE-6  |1=INHIB.
 0000 0000 0000 0000 0000 0000  |----ABCD
     --END OF SECTION--
```

No overlaps are inhibited, all overlaps will operate normally in all pre-empt sequences.

ENTRY TIMINGS...(PRIOR MENU)...Selection 3...

```
    --PE ENTRY TIMINGS INPUT #1--
MGR WLK PCL OLY OLR FDW/Y | USED FOR PE
  5   1   7   4   2  OFF  | ENTRY ONLY
   (0-9.9 OR 127)  (OFF/ON)
```

PG DWN, etc....same for inputs 2-5, but sequence 6 is as follows....

```
    --PE ENTRY TIMINGS INPUT #6--
MGR WLK PCL OLY OLR FDW/Y | USED FOR PE
 22   0   0   4   2  OFF  | ENTRY ONLY
   (0-9.9 OR 127)  (OFF/ON)
```

The first 5 sequences use low values so that the response is rapid. Sequence 6, however (soft flash sequence), uses different values. The reasoning here is that there is *no hurry to* get to soft flash. In fact, notice that the minimum green is set at 22 seconds and WALK and PCL are set to 0 (0= use normal settings). This would Indicate that the phase can time normally, with extensions up to 22 seconds before pre-empting. If the phase gaps out before then, it will proceed directly to pre-emption after extensions, after clearing.

PRIORTIES...(PRIOR MENU)...Selection 4...

```
    --PRIORITY OF PE SEQUENCES--
INPUT 1 2 3 4 5 6 | PRIOR 1-6, USE SAME
PRIOR 2 2 2 2 1 3 | NO. FOR ALL W/SAME.
FL/OV 1 1 1 1 1 0 | FL/OVER:1=OVERRIDE
```

The priorities are arranged such that input 5 (Railroad) has the highest priority and will override all others. The 4 fire run sequences are next highest, but are all the same with respect to each other, i.e. first come first serve.

Pre-empt input #6 (soft flash) has the lowest priority. All sequences except 6 will override remote flash.

HOLD ONLY...Selection 5...

```
INPUT     1   2   3   4   5   6  |ON=HOLD
ON/OFF  OFF OFF OFF OFF OFF OFF  |ONLY, NO
PHASES                           |PE SEQ.
TIME      0   0   0   0   0   0  |REQUIRED
```

None of the sequences have been programmed as "Hold Only", thus, they are all "sequence" type pre-emptors.

DELAY OPTION...Selection 6...

```
 --OMIT DURING DELAY BEFORE PE OPTION--
   DELAY B4 PE #    1   2   3   4   5   6
PED OMIT LAST X   18  18  18  18   0   0
VEH OMIT LAST X   10  10  10  10   0   0
```

Note that since there is no delay before pre-empt timing *currently* programmed, this feature would have no effect However, if delay before pre-empt timings were programmed for sequences 1-4, this feature would operate such that all peds would be omitted during the last 18 seconds of the delay and all non pre-empt phases would be omitted during the last 10 seconds of the delay period.

PRE-EMPT MAPPABLE INPUTS AND OUTPUTS

PRE-EMPT NO-DELAY INPUTS (PND1-6)

These correspond to normal PE inputs 1-6 except that they are always immediate and ignore any delay before pre-empt programming. PEND inputs are most likely used in dual switch pre-empts where the normal PE input detector is placed upstream and has delay with delay option (omit last X) timing. The PEND input detectors are then placed near the intersection for "hard pre-empt". The upstream input (normal PE) thus "preps" the intersection for the "hard PE" to come from the PEND input. Any residual delay timing is simply ignored when the PEND input detector is hit.

PRE-EMPT ACKNOWLEDGE OUTPUTS 1-6

These correspond to PE inputs 1-6 to indicate the pre-empt call is received. These outputs activate upon first receipt of the corresponding PE call, *even during the delay period.* Typically used where it is critical that the pre-empt switching system receives positive feedback that the signal has been acknowledged.

NOTE ABOUT USE OF MAPPABLE FUNCTIONS

Pre-empt no-delay and pre-empt acknowledge are I/O "functions" and are not assigned to physical pins from the factory. These can, however, be assigned to any pin in the I/O configure programming section. Available pins must be created by mapping the desired function in place of unused functions. See section XI.

89 CODE "GAP TIMER" FEATURE

Allows the PE step time to act as gap timer. The 89 code would be placed in the step following the pre-empt hold phases. The 89 step would have timing like a passage timer, say 2-8 seconds, and HOI would be OFF. The previous hold phase step would have normal timing and HOI = ON (see note). The "89" step holds at full value if the input is present, times down if the input goes away and sets back to full value if the input comes back before time-out....like a passage timer. The previous step's phases are maintained until the input goes away, the gap timer times out, and the unit advances out of the "89" step.

Note: When using the "89" gap timer step for normal non-priority return pre-empts, it is not necessary to turn *HOI= ON* for either the pre-empt phase step or the next "89" step since the "89" step itself will act like a hold step with gap timing. However, when using priority return pre-empt, particularly with the Skip Option = ON, **HOI must be programmed ON** for the pre-empt phase step. The unit uses the HOI = ON step to recognize the "pre-empt phase(s)". The "89" step **may or may not** have HOI = ON.

PRIORITY RETURN PRE-EMPT FEATURE

When this feature is in effect, the LMD9200 software keeps track of the phases that are forced to terminate upon entry into pre-emption. if the percentage green time of the terminating phase green (or ped clearance) is less than a user settable minimum amount, the LMD9200 can return directly to that phase or phase pair upon execution of the "95" pre-empt instruction. If it does not return to the terminated phases it returns to the *next phase(s)* after those. The feature is intended to provide more equitable service when normal sequencing is frequently disrupted by pre-emptions.

BASIC FEATURES and DESCRIPTIONS

The phase percentage green is computed relative to user settable values. These values pertain to Max times if the controller is in free operation, and coord auto-calc split values if running coordinated.

A feature to enable skipping of the just-served pre-empt phases (skip one cycle after pre-empt) following the priority return phases is available as an option.

Four sets of time-of-day selectable phase minimum percentage threshold values and a time-of-day priority return inhibit feature are available (in case priority return is not desired during off-peak hours). These time clock functions are circuits 66-69 which have special operation when the priority return mode is on, as follows:

Active Clock ckt	Normal Function	Function when P-Return = ON
None	N/A	Select PRA min %'s
66	PE1 call	Select PRB min %'s
67	PE2 call	Select PRC min %'s
68	PE3 call	Select PRD min %'s
69	PE4 call	Inhibit priority return

When priority return is inhibited, the 95 instruction is simply skipped in the sequence.

A separate set of ped minimum percent thresholds is available for monitoring ped clearances. If the ped clearance is shortened below the settable threshold, the unit will priority return back to walk of that phase. The ped threshold takes precedence over the phase threshold.

Note: To enable priority return to peds, The "93" code (which enable peds during pre-empt) must be executed prior to the 95 code to get ped service on the initial priority return service. This is because the unit is effectively still in pre-emption when "95" is executed. Otherwise, the ped call will be placed but will not be serviced until the next time around in the normal sequence to that phase.

2. The set-up screens for priority return are as follows:

HI PE SET-UP.....

```
          --PE SET-UP--
1.MEM/DEL/RESVC 4.PRIORITIES 7.PRIOR RET
2.O/L INHIBITS  5.HOLD ONLY
3.ENTRY TIMES   6.DELAY OPTION
```

PRIORITY RETURN....

```
      --PE PRIORITY RETURN--
  MODE: ON | ON = PRIOR RET MODE
OPTION: ON | ON = SKIP PE PHASES
                  1ST CYCLE AFTER PE
```

Mode: OFF = Priority return pre-empt is disabled.
ON = Priority return pre-empt is enabled.

Option: OFF = No phases skipped after pre-empt
ON = Pre-empt phase(s) skipped once after pre-empt if unit priority returns to phase(s) just preceding. For example, if 2 & 6 are the pre-empt phases and the unit priority returns to 1 & 5, then 2 & 6 are skipped the first cycle after pre-empt.

PG DN.....

```
--95 PRIORITY RETURN PHASE MIN PERCENTS-
 PHASE   1   2   3   4   5   6   7   8
 PRA %   60  60  60  60  60  60  60  60
 PRB %   40  40  40  40  40  40  40  40
```

If a phase is served below these thresholds before exiting for pre-empt, the phase will be priority served after pre-empt. If the phase is served over the threshold, the next phase after it will be served. These values pertain to Max times if the controller is in free operation, and coord auto-calc split values if running coordinated.

PG DN for PRC & PRD, then once again for ped percents....

```
 --PED PRIORITY RETURN MIN PERCENTS-
PHASE   1   2   3   4   5   6   7   8
PED %  80  80  80  80  80  80  80  80
```

If the phase is pre-empted during walk or ped clearance and the ped clearance is shortened below the settable threshold, the unit will priority return back to walk of that phase. The ped threshold takes precedence over the phase threshold, i.e. the ped priority return can take place even if the phase threshold has been satisfied (if the ped hasn't). There is only one set of ped thresholds (one for each phase). This set is active for any of the time clock selected phase thresholds.

EXAMPLE USING 95 PRIORITY RETURN CODE

1. Set up the Priority return option using the values shown in this section for an 8 phase dual ring controller.

2. Note that auto-calc values must be entered if the priority percentages shown on this page are to operate on coordination split timing. The priority percentages operate on Max times in free operation.

3. Set up the sequence 1 steps as shown below. ***This example also uses the 89 gap timer feature***.
MM-2-5-1....

```
SEQ1|PHS-SPECL|TIME|HOI  |PE-OUTS|90=RED
  1 |26       | 7  | ON | 1     |99=RET
  2 |89       | 3  |OFF | 1     |.1-.9=
  3 |95       | 1  |OFF |       |SPEC'L
```

Pg dwn....

```
SEQ1|PHS-SPECL|TIME|HOI  |PE-OUTS|90=RED
  4 |99       | 0  |OFF |       |99=RET
  5 |         | 0  |OFF |       |.1-.9=
  6 |         | 0  |OFF |       |SPEC'L
```

Operation

1. The unit will pre-empt to phases 2 and 6, keeping track of how much of the pre-empted phase time was served prior to pre-empt. For example, say PRA %'s are in effect. Then if the controller running free operation and phase 4 and 8's max times are 30, then the threshold for 4 and 8 is 60% of 30 or 18 seconds. If served more than 18 seconds when pre-empted, then 4 and 8 won't get priority return service. If less than 18 seconds are served, they will.

2. Note that the gap time feature is being used in the second step (89 code). The first step is the hold step and the second is the gap. The unit pre-empts to 2 and 6 and holds for at least 7 seconds, and longer if the input is maintained. If the input goes away for a moment, it proceeds to step 2. The same phases (2 & 6) are maintained in step 2 as in step 1. If the input comes back before the 3 seconds times out in step 2, the timer resets. If not, it proceeds to step 3. Note that the guaranteed pre-empt time (in the case that the input is already gone) for phases 2 & 6 is 10 seconds, 7 in step 1 and 3 in step 2.

3. The third step is the 95 return step. The unit will make a decision in this step as to whether or not to priority return to the originally pre-empted phase.

4. The fourth step is the 99, "return to normal operation with calls" instruction. Code "98" (no calls) could have been used here as well.

5. Note that since the skip option is on, if the unit priority returns to the phases directly preceding the pre-empt hold phases (phases 1 and 5 in this case) then 2 and 6 will be skipped after service to 1 and 5. They are only skipped that first cycle after pre-empt. Normal operation resumes after that.

TRANSIT PRIORITY OPERATION

INTRODUCTION

The following descriptions relate to the Transit Priority feature set in the LMD9200 which provides enhanced service to transit vehicles. The operation is initiated by a special call placed into the controller unit such that;

1. If not in the transit priority phase, the LMD9200 will time intermediate phases a little quicker than normal to get to the *transit priority phase(s)* sooner than normal.

2. Once achieved, or if already in the transit priority phase(s), the LMD9200 may *extend* the transit priority phase(s) a little bit longer than the normal phase max or split time if needed. Note that normal max timing includes normal max 1 or 2, max plans, or fail max timing—whichever is in effect.

3. Inputs may operate in a single detection presence mode (constant call) or a two detector "check in, check out" mode. In this mode, an upstream detector places a call in memory which is then cleared by a far side detector once the vehicle has cleared the intersection.

Other than its priority service, the transit priority phase is just a normal phase used for general vehicles. Each transit priority service is in response to a special input designated for that purpose. Transit priority is not pre-emption, and is not intended to be as aggressive in nature. It does not skip phases nor disrupt coordination as severely as pre-emption typically does.

TRANSIT PRIORITY INPUT MAPPING

-Transit priority service is called for by mappable inputs designated TP1-6 for priority transit priority 1-6.

To use the transit priority feature, these must be assigned (mapped) to actual pins as needed.

-To do so, choose available pins that are not needed for another function and map them accordingly. Be sure to zero out the pin assignment to the unneeded function so it will not be falsely activated. See I/O mapping, page 11-3.

Note that:

1. CUSTOM MAPPING must be toggled enabled, and

2. LOAD I/O CONFIG CHANGES must be executed after assigning transit priority pins.

TRANSIT PRIORITY INPUT SCREENS

I/O configure area, custom I/O mapping, input mapping.

Main Menu-4-2-3-page down 23 times.....

TPr1	TPr2	TPr3	TPr4	TPr5	TPr6	TPrI
152	233	0	0	0	0	0
OR	OR	OR	OR	OR	OR	OR
0	0	0	0	0	0	0

Note: Pins shown are normally ph 1 & 3 ped omits

TPr1-TPr6 = Transit priority *request* inputs 1-6
TPrI = Transit priority *Inhibit* (all request inputs)

Pg dwn.....

TPC1	TPC2	TPC3	TPC4	TPC5	TPC6
0	0	0	0	0	0
OR	OR	OR	OR	OR	OR
0	0	0	0	0	0

TPC1-TPC6 = Transit priority *clear* call from memory inputs 1-6

Pg dwn....

TIP1	TIP2	TIP3	TIP4	TIP5	TIP6
0	0	0	0	0	0
OR	OR	OR	OR	OR	OR
0	0	0	0	0	0

TIP1-TIP8 = Phase 1-8 conditional transit priority shorten *INHIBIT* inputs

INPUT DEFINITIONS

TPr1-TPr6. These call the TP process for the assigned phases *(phase assignment and timing in transit priority set-up programming*). Once the transit priority phase has been achieved, it will hold until the input goes away or the transit priority maximum extend period times out.

TPrI. This is an **unconditional transit priority inhibit input**, When activated, ***all*** transit priority inputs are inhibited (no transit priority allowed).

TPC1-TPC6. Transit priority memory clear inputs. Each clears its corresponding call from memory (it also disables the request input when active). Typically used with two detector systems where the first is placed on the near side of the intersection using a TPr (request) input with memory set to on. The second is on the far side of the intersection and uses a TPC (clear call) input to clear the call once the vehicle is through the intersection.

TIP1-TIP8. Phase conditional transit priority shorten inhibit inputs, When activated, Transit Priority can not shorten the corresponding phase if the phase is not the TP phase. The phase, however, can be the TP phase and can be extended.

TRANSIT PRIORITY CALL DETECTION AND INITIAL OPERATION

When mapped**,** the transit priority call inputs are constantly monitored for activity along with the general controller inputs. When a transit priority call is detected on any of the inputs, to ensure transit priority phase service, a standard vehicle call is applied to the assigned transit priority phase(s) for the duration of its activity. All other ped and vehicle calls are allowed normally. ***The process can operate in either free or coordination mode.*** Depending on programming, special timings such as special maxes and walks from TP group programming are used until the transit priority phase(s) are achieved. A priority system may be implemented if more than one TP input is to be used. Higher priority inputs override lower priority inputs. If all of equal priority, the first transit priority phases to become active from any of the active inputs will be considered "achieved" and will cause the unit to hold at that point.

TRANSIT PRIORITY SET-UP PROGRAMMING

From the Program/Read mode menu....

```
          --PROGRAM/READ MODE--
1.SECURITY CODE 4.TIME CLOCK   7.REPORTS
2.CONTROLLER    5.PRE-EMPTION  8.TRANSIT
3.COORDINATION  6.COMM SET-UP
```

TRANSIT.....Selection 8....

```
     --TRANSIT PRIORITY SET-UP--

1.TP INPUT SET-UP   3. TP FREE MODE
2.TP GRP TIMING     4. TP COORD OPTIONS
```

TP INPUT SET-UP.....Selection 1....

```
    --RANSIT PRIORITY INPUT SET-UP--

1.PHASES/MEM/DEL     3.INPUT PRIORITY
2.INPUT TIMINGS
```

PHASES/MEMORY/DELAY.....Selection 1....

```
TP INPUT   1    2   3   4   5   6
PHASES    26   48   0   0   0   0
DELAY      0    0   0   0   0   0
MEM      OFF  OFF OFF OFF OFF OFF
```

PHASES = The desired TP phase(s) for that input to go to (up to 4 phases). Transit priority phases may or may not be the coordinated phase(s).

DELAY = 0-255 seconds. The desired delay from activation of an input to its response.

-If memory is off, the input must remain steady active through the delay, or TP will not occur. The delay timer resets and must start over on each new input activation.

-If memory is on, the delay will continue to time through to the TP sequence once a call is placed, even by an input pulse. The delay timer will reset only if the call is cleared from memory.

MEM ON = The input call will latch and remain active until either cleared by the clear input, the "Maximum Wait" value times out, the "Max Extend" timer times out, the "input fail" timer times out, or the inhibit (all) input is activated.

MEM OFF = The input call will go away as soon as the input does (not latched).

TP INPUT TIMINGS....Selection 2....

```
TP INPUT   1    2   3   4   5   6  ALL
MAX WAIT  60   30   0   0   0   0
MAX EXT   12   10   0   0   0   0
MIN RSVC   0    0   0   0   0   0   5
```

MAX WAIT = Maximum Wait (0-255 seconds). This value begins timing upon activation of the input. The timer times down as long as the input remains active or a call remains in memory. If the Max Wait timer times out before the transit phase is achieved, the input is disabled and/or the call is cleared and Transit Priority is canceled. The input remains disabled until the input goes away.

Note: A zero max wait value is considered "max wait inhibit" and max wait will be ignored for that input. True max wait values are then 1-255 secs.

INPUT FAIL TIMER (non-programmable)

There is a non-programmable 255 second timer which also starts timing along with the maximum wait timer (but is likely much longer than max wait). If the fail timer times out, the input is considered failed (stuck on) and will be recorded as such. No further transit priority service is allowed on that input until the input goes away and clears the failure (and also clears max wait fail). The difference between this and the max wait timer is one of degree and the associated report logged. An input failure would typically warrant field service, unlike the more routine max wait cancellations.

MAX EXT = Max Extension Time (0-255 seconds). This value establishes the time in seconds that the transit priority phase can extend beyond its normal max or force off. A value of 0 disallows extension. The transit priority max extension timer begins timing only when the transit priority call is still active and the transit priority phase would otherwise normally terminate either by max-out or force off (when coordinating). The unit resumes normal timing if the max extend timer times out, even if the Transit Priority input is still active. Max extend typically occurs when the transit priority call arrives late in the normal TP phase. Max extend timing during coordination will *hold the cycle timer in place** and will release it when it times out or the input/call goes away. Offset seeking will result.

***The purpose for holding the cycle timer** in place is so that the cycle timer does not *get ahead* of the phasing--which tends to cause subsequent phases to short time. Holding the cycle timer will indeed cause it to be out of sync and results in offset seeking, but this is usually far less detrimental to traffic than short timing phases.

LIMITS ON MAX EXTEND DUE TO PRE-EXISTING OFFSET SEEKING CONDITIONS

Shortway offset seeking is a process in which the local timer adjusts itself to get "in sync" to the master cycle + programmed offset. It involves timing the local cycle timer either "fast" or "slow" by 20% as needed. It seeks fast if the local cycle is behind schedule, and seeks slow if it is ahead of schedule. This process is routinely used in the normal operation of coordination to achieve sync. Transit priority can only stop the cycle timer during TP max extend timing--which will make it further behind where it currently is. As a result, the only affect it can have on offset seeking is to cause it to start seeking "fast" if not already doing so, or to seek fast for a longer time if already doing so.

The TP process takes any pre-existing offset seeking into account by modifying the programmed max extend timer. The modified value is called the ***allowed extend value***. This value is determined by computing how far ahead or behind of sync the unit currently is:

-If already behind and thus seeking fast, the max extend period may be *reduced*. For example, if the actual local offset is greater* than the programmed offset by 6 then the local cycle is behind by 6 and is seeking fast. If the programmed TP max extend is say 10, then only 10-6 or 4 seconds of actual extend time will be allowed.

*Allowing for cycle roll-overs a local offset of 6 would be considered "greater" than 89 in a 90 second cycle.

-If already ahead and thus seeking slow, the extend period may be *increased*--***but not to more than a built in limit of 1.5 times the programmed extend value.*** For example, if the actual local offset is less than the programmed offset by 6, then the local cycle is ahead by 6 and is seeking slow. Say the programmed TP max extend is 10, then 10 + 6 = 16 seconds would be computed, but this is greater than 1.5 x 10 = 15. The resulting max extend time would then be 15 seconds.

Note that the TP max extend values are used strictly as they are programmed during free operation, i.e. a TP phase in free operation can unconditionally extend up to its programmed max extend value and no more.

MIN RESV:

Inputs 1-6 = Min Re-service, inputs 1-6 (0-99 minutes). This value specifies the minimum time before any two successive priority transit service calls are allowed on the same input.

ALL = Min Re-service, all inputs (0-99 minutes). This value specifies the minimum time before any two successive priority transit service calls are allowed in general, regardless of input.

NOTE: The min re-service function has a built in 5 second recognition timer, i.e. the input (call) must be active for 5 consecutive seconds to enable the min re-service timer. This prevents a slightly intermittent detection system from being locked out because of a brief loss of signal.

INPUT PRIORITY....**Selection 3....**

```
 TP INPUT    1   2   3   4   5   6

PRIORITY     1   2   3   3   3   3
```

INPUT PRIORITY CODES: 1 = Low, 2 = normal, 3 = high (controller may show 0's if never programmed, 0 is the same as 1 functionally)

Assign values of 1-3 to each TP input. Inputs of higher priority will override those of lower priority. Inputs of the same priority will be served concurrently, where the first TP phase achieved will TP hold, then go on to the next, etc.

Note that a higher priority TP input will cease overriding lower priority inputs if it's max wait or fail timer times out.

TRANSIT PRIORITY GROUP TIMING

Transit Priority Group Timing is used to time out non-TP phases quicker when going to a TP phase. Once the TP phase(s) is achieved, the normal selected timing resumes, i.e. group timing is not used for the TP phases themselves.

PRIOR MENU.....

```
      --TRANSIT PRIORITY SET-UP--

1. TP INPUT SET-UP  3. TP FREE MODE
2. TP GRP TIMING    4. TP COORD OPTIONS
```

TP GRP TIMING....Selection 2....

```
    --TRANSIT PRIORITY GROUP SET-UP--

1. GRP MAX TIMES
2. GRP WLK TIMES
```

GRP MAX TIMES...Selection 1....

```
PHASE      1   2   3   4   5   6   7   8
GP1 MAX   22  18   0   0   0   0   0   0
GP2 MAX   26  20   0   0   0   0   0   0
GP3 MAX   30  22   0   0   0   0   0   0
```

Range; 0-255 seconds

There are three sets of group max times and one max time per phase per group. When the group is selected by Free Mode or CS assignment, the associated group max time will determine *shortest max time allowed* for non-CNA phases when attempting to time out that phase quicker to get to a transit priority phase. These max values are typically set shorter than the normal max or split time* The values are used directly during TP transition in free operation, but are only a part of a more complex computation involving *cycle leading limits* during coordination (see max value computation during coord below).

****In coordinated operation, the normally used*** max is typically set long enough so that the phase will force off before maxing out. In the case of going to a transit priority phase, the group maxes would be set up to be shorter than the split time so non-transit priority phases will be allowed to ***max out before forcing off***.

The purpose for several groups is so that different value TP max times can be used with different cycle split combinations.

TP MAX VALUE COMPUTATION DURING COORDINATED OPERATION:

Under TP control during coordinated operation, the max timer values of non-TP phases are actually computed in consideration of both the ***GRP MAX TIME*** and the ***CYCLE LEADING LIMIT*** (see cycle leading limit set-up). Upon activation of a non-TP phase while an input is active, the unit will attempt to compute an appropriate max time such that it will time out *exactly at the cycle leading limit threshold point (force off minus leading limit value).* However, it applies the restriction that this value *cannot be less than group max time.* Thus, the longer of these two concerns takes precedence. If the phase has not begun timing, the max is initialized to the computed value on phase start up. If it is already timing, the max timer is dynamically corrected.

Example of TP MAX value computation

Say for a non-TP phase about to be terminated due to a TPr input (for another phase);

- -The phase's normal max value is 30
- -The phase's selected TP GP max is 15.
- -The phase normally forces off at 60 seconds (in the active cycle/split)
- -The *cycle leading limit* for the active TPr input is 10 seconds (the cycle leading limit threshold is then at 50 seconds since the force off is at 60).

-Scenario 1. Say when the transit priority input becomes active the current cycle timer is at 55 while the phase's max timer is at 20 (max timers time down).

Since the threshold of 50 has already been obtained, the leading limit computation would want to set the max timer to 0 (actually 1 is the lowest value it will load). However, since the max timer has timed only 10 seconds (30-20), the group max timing computation will want to set it to 5-- meeting the group max time requirement of 15 seconds total green. Since 5 is higher than 0, the max timer will change its current value of 20 to 5.

-Scenario 2. Say the current cycle timer is only at 40 while the phase's max timer is (as above) at 20. Since the threshold of 50 will not be obtained for 10 more seconds, the leading limit computation will want to set the max timer to 10. Since the group max timer computation will only want to make it 5 (as in scenario 1), the cycle leading limit's value of 10 takes precedence. The max timer will change its current value of 20 to 10.

TP GROUP WALK TIMINGS....Selection 4....

PHASE	1	2	3	4	5	6	7	8
GP1 WLK	7	7	0	0	0	0	0	0
GP2 WLK	7	9	0	0	0	0	0	0
GP3 WLK	7	10	0	0	0	0	0	0

Range; 0-9.9 or 0-127 seconds

The TP walk group times operate similarly to the TP max group times, including dynamic adjustment*. These are typically set shorter than normal walk (particularly for phases with long walk times) and will be generally used to time out the phase walk quicker to get to a transit priority phase. The group assignment to cycle and split is the same as for TP Max groups, i.e. a group assigned to a C/S combination pertains to both max's and walks. ***See TP group walk timing computation during coordination below.***

**TP group walk times with zero values will be rejected* relative to dynamic adjustment. That is, once a walk has started normally, it cannot be adjusted to a zero value, but will time out normally. Zero values for walks that have not started, however, will be treated as a form of ped omit and the walk will be skipped.

Note that Cycle Leading Limits should be employed for CNA coord phases so that the transit priority process will *not initiate the release of hold too early* (see cycle leading limit programming).

Ped clear is not included in any TP groups because it is not prudent to reduce ped clear times simply for transit priority (TP is not pre-emption).

TP GROUP WALK TIMING COMPUTATION DURING COORDINATION:

TP Group walk timing is straightforward, whether coord or free, the walk is simply re-computed to reflect the TP group time with no other considerations. When cycle leading limits are applied for CNA coord phases, however, walk may hold after the group walk time times out. The CNA walk will then hold until the normal phase force off point minus the cycle leading limit value. If this threshold has already been surpassed when the group walk time times out, the phase will immediately begin ped clear.

Note: The hold duration described above is based on a ***CNA coord phase force off*** value being judiciously programmed. The correct placement of the CNA force off point is at the desired release of walk point, which can also be considered the desired end of phase green minus ped clear.

TP FREE MODE

Back to the transit priority set-up menu...

```
      --TRANSIT PRIORITY SET-UP--

1. TP INPUT SET-UP  3. TP FREE MODE
2. TP GRP TIMING    4. TP COORD OPTIONS
```

TP FREE MODE....Selection 3....

```
 --TRANSIT PRIORITY MODE IN FREE OP—
 MODE  | 0   = USE SHORTEST OF MX1 OR
   0   |       MX2 & STANDARD WALKS
       | 1-3 = USE MAX/WLK GP 1-3
```

This option determines how the Transit Priority will operate when the unit is in free operation (no coord).

Mode = 0 The Transit priority process will select the shortest of max 1 or max 2 for each phase when attempting to shorten the phase to get to a transit priority phase. Normal walk times only are used (no walk reductions).

Mode = 1-3 The Transit priority process will select the indicated group 1-3 when attempting to shorten the phase to get to a transit priority phase. The selected group applies to both the TP max time group and the TP walk time group (e.g. group 1 = group 1 max's and group 1 walks). Program these accordingly

TRANSIT PRIORITY COORD OPTIONS

This menu provides optional programming related to coordinated operation

Selection 4....

```
   --TRANSIT PRIORITY COORD OPTIONS--
1. CYC & SPLIT  TO  TP  MAX/WLK  GPS 1-3
2. PRE TP CYCLE LEADING LIMITS
3. POST TP MAX EXT'S UNTIL FIRST FO
```

CYCLE & SPLIT TO MAX/WLK GP 1-3 Selection 1....

```
 --CYCLE AND SPLT TO TP MAX/WLK GP 1-3
CYC       1   2   3   4   5   6   7   8
SPLT1/2 1/1 2/2 3/3 0/0 0/0 0/0 0/0 0/0
SPLT3/4 1/1 2/2 3/3 0/0 0/0 0/0 0/0 0/0
```

The example screen shows group 1 assigned to all cycle 1 splits, group 2 to all cycle 2 splits and group 3 to all cycle 3 splits.

For each cycle and split, assign the desired TP group 1-3 to be used when that cycle/split is in effect. The assignment pertains to both max and walk groups (e.g. group 1 = select both group 1 max's and group 1 walks when that cycle/split is in effect).

PRE TP CYCLE LEADING LIMITS.....Selection 2.....

```
 - LIMIT PH'S CAN GET AHEAD OF CYCLE -
PHASE     1   2   3   4   5   6   7   8
LIMIT    12  15   0   0   0   0   0   0
  (0 = NO LIMIT, 1-255 LIMIT IN SECS)
```

LIMIT: 0 = Not used, no limit

1-255 = Maximum number of seconds ahead of force off phase is allowed to terminate under TP control

Used for coordinated operation, these values limit the amount that any individual phase can be shortened relative to its force off point within the cycle timer. The TP group max times also affect phase timing in con-junction with these values--see the discussions on *TP max and walk value computations during coordinated operation*.

The cycle leading limits have the following effects :

-For any CNA coord phase it prevents hold from being released too early and thus causing a short timed phase (usually the major street). **Note:** The user must program CNA coord phases to force off at the yield point (end of walk) for this to work properly--not the end of green.

In two phase operation the limit values may used to protect against cases in which phases are somehow allowed to start very early and it is not desired to have them terminate correspondingly early. For two phase operation, however, the TP group Max timings alone will generally determine how far ahead of the cycle the phase can get since the unit can only be in one other phase besides the TP phase. There is no theoretical *accumulation* of earliness. It is still not a bad idea to use leading limits in this case.

-In multi-phase operation (3 or more phases) the limit values do prevent the accumulation of individually shortened times to get to such a magnitude that latter phases get too far ahead of the cycle.

Note that the limit values only restrict the ability of the Transit Priority process to cause a phase to terminate too early. Actuated phases *can always gap-out*.

POST TP MAX EXT'S UNTIL 1ST FO

This option adds a value called the **POST TP MAX EXT time** to the normal max time of all non-CNA phases once the TP phase has been achieved. This process occurs only at the beginning of each phase when the max timer is initialized (no dynamic adjustment). Once started, it will continue to do so until some (any) force off occurs.

Selection 3.....

```
 POST TP PH MAX EXT'S UNTIL 1ST F.O.-
PHASE     1   2   3   4   5   6   7   8
MAX EXT  10  10   0   0   0   0   0   0
AUT EXT OFF  ON OFF OFF OFF OFF OFF OFF
```

The feature can be used to protect against ***early phase max-outs following transit priority*** service. This may be required when phases, including and especially the TP phases themselves, are served significantly early due to the TP process. This is likely to occur when a queued TP vehicle calls for service, compels other phases to leave early, and then gets right through when the green comes. Under such circumstances without this option; since the phase would start early, it may max out early as well (relative to its force off). This could be detrimental to progressions in coordinated operation, especially for grid systems where side phases are also

likely to be coordinated. There is no coord "hold" applied to such phases to prevent early max-outs. Once a force off occurs, the process is no longer required because phases are theoretically back in step with the coordinator at that point.

POST TP MAX EXT VALUES.

0 = There is no additional time, phases will use their normal max times once the TP phase has been achieved.

1-255 = The additional post TP max time extension in seconds. For example, if MAX EXT = 10 and the normal max is 30, then the phase max timer will be initialized to 40 when in effect (i.e. after TP phases have been achieved).

NOTE: Post TP ***MAX EXT*** times should not be confused with the **GROUP MAX** times. Group max times are used when "going to" TP phases and are typically set up to shorten the normal max's. MAX EXT times are set up to add max time to prevent early max outs *after TP phases have been achieved early*.

AUTO EXTEND FEATURE

Used to automatically call and extend actuated phases after transit priority service ends until the first force off occurs in either ring. Prevents actuated phases from not receiving a call or gapping out before the platoon arrives due to early service as a result of TP.

OFF = No auto extend
ON = Phase is called and extended after TP occurs

POST TP MAX EXT AND AUTO EXTEND NOTES

1. These functions are intended for coordinated operation only. The options are not used during free operation.

2. The MAX EXT feature applies to only to non-CNA phases (actuated, ped recall, or recall max).

3. Both options are disabled ***when the first force off following a transit priority occurs***. A force off being issued (in either ring) is an indication that the phases are back under control of the coordinator and these special options are no longer required. Once disabled, the features are not re-invoked until after another Transit Priority event.

TRANSIT PRIORITY RUN (STATUS) SCREENS

BASIC STATUS SCREEN
This is screen initialized by hitting ***RUN STATUS***.

NORMAL MODE. When no priority transit priority is active, the display indicates normal operation, such as normal coordination shown below....

```
PHASE/OL 1 2 3 4 5 6 7 8 A B C D| CYCLE
SPO      r G r r r G r r r r r r| 1  90
MIN  4   WLK  5 |MIN  4   WLK  5| OFST
MX1 16   PSG  3 |MX1 21   PSG  2| 1  10
```

TRANSIT PRIORITY INPUT ACTIVE. Activity of a transit priority input is shown in the lower right corner. One or more transit priority inputs may be active (up to 6)....

```
PHASE/OL 1 2 3 4 5 6 7 8 A B C D| CYCLE
SPO      r G r r r G r r r r r r| 1  90
MIN  4   WLK  5 |MIN  4   WLK  5| TPR
MX1 16   PSG  3 |MX1 21   PSG  2| 1
```

ALTERNATE TIMER SOURCE INDICATIONS.

While going to a transit priority phase, alternate timing may be employed (alternate max or Transit priority Group 1-3). The source of such timing will be appropriately displayed.....

```
PHASE/OL 1 2 3 4 5 6 7 8 A B C D| CYCLE
SPO      r G r r r G r r r r r r| 1  90
MIN  4   WLK  5 |MIN  4   WLK  5| TPR
TG1 12   PSG  3 |TG1 14   PSG  2| 1
```

Note that in this example, The walk and max times are derived from Transit Priority Group 1 and are so indicated.

TRANSIT PRIORITY PHASES ACHIEVED. When the transit priority phase associated with an active input has been achieved in a ring, the screen indicates.....

```
PHASE/OL 1 2 3 4 5 6 7 8 A B C D| CYCLE
SPO      r G r r r G r r r r r r| 1  90
MIN  4   WLK  5|MIN  4   WLK  5| TPR
MX1 16   TPR PHS|MX1 21  TPR PHS| 1
```

TRANSIT PRIORITY EXTENSION TIMER

When the transit priority phase has timed its max or to its force off point, yet the input remains active, the transit priority extend timer begins timing down and is displayed....

```
PHASE/OL 1 2 3 4 5 6 7 8 A B C D| CYCLE
SPO      r G r r r G r r r r r r| 1  90
MIN  4   TPX   7|MIN  4  TPX   7| TPR
MX1 16   TPR PHS|MX1 21  TPR PHS| 1
```

NOTES;

1. The cycle timer stops when transit priority extend is timing.

2. The Max extend timer starts timing down when phase would otherwise terminate

Note that the extend timer immediately clears and the phase terminates if the call clears. Also note that during coordinated operation, the cycle timer *stops* when the transit priority extend timer is timing. This prevents the cycle timer from getting too far ahead of the phasing which could result in very short timing of down stream phases. Instead, it stops until the transit priority phase is released, then starts up again and immediately begins offset seeking.

TRANSIT PRIORITY INPUT AND TIMER RUN SCREENS

The following menus and status screens pertain to Transit Priority inputs and related timers. Go to Basic run status menu (MM-1).....

"N/A" if not TS2 mode

```
        --BASIC STATUS MENU--
1.RUN MENUS    4.PREEMPT    7.MMU STATUS
2.FAULTS       5.MOE STATUS 8.TRANSIT PR
3.CLOCK STATUS 6.SCHED LOGS
```

TRANSIT PRIORITY....Selection 8,

CALL/DELAY/MAX WAIT TIMERS.....

```
         TPR1 TPR2 TPR3 TPR4 TPR5 TPR6
CALL        F    M
DEL         0    0    0    0    0    0
MAX WAIT   60   22    0    0    0    0
```

The TPR input status definitions are as follows:

CALL: Blank = Input not active
X = Input active, transit priority in process
M = Call stored in memory
CW = The input is active but is canceled due to max wait time out (note 1)
DC = The input is active but is disabled by the clear call input (note 2)
DP = The input is active but is disabled due to a higher priority input
DR = The input is active but is disabled due to min re-service
d = The input is active but the delay timer is timing
F = The input is active but is failed due to the 255 second fail time out (failed until input goes away).
DI = All inputs disabled due to the inhibit input (note 3)
PE = The input is active but the unit is in pre-emption

Notes:

1 . The max wait timer also times down when there is a call in memory, even if the input is not active. The call, however, will *automatically be cleared* if the max wait timer times out before the call is cleared by the normal clear input. As a result, the TPR (call) input must remain active for the CW indication to be displayed.

2. The clear call input clears the call stored in memory, but also *inhibits* its associated TPr input while active.

3. "DI" will always appear beneath ***all 6 TPR inputs*** when the inhibit (all) input is active regardless of TPr activity.

DEL: 1-255 = Delay timer timing (times down)
0 = Delay timer not timing or timed out

MX WAIT: 1-255 = Max Wait timer timing (down)
0 = Max Wait timer not timing or has timed out

FAIL AND RE-SERVICE TIMERS

Pg dwn from Call/Delay/Max Wait timer screen.....

```
TMR     TPR1 TPR2 TPR3 TPR4 TPR5 TPR6
FAIL     255  255  255  255  255  255
RSVC       0    0    0    0    0    0
RSVC ALL   0
```

FAIL TIMER: This timer value is fixed at 255 seconds and times down whenever the input (or call in memory) is active. The timer resets (to 255) when the input goes away or the call is cleared. If it times out, the input is declared failed. Note that if there is a call only in memory (memory on, input has come and gone), the call will be cleared when the *max wait* timer times out. Thus a call in memory should not cause an input fail unless max wait is set to 0 (inhibited) or 255 (the same as fail).

RSVC TIMER: These are the per input re-service timers. If programmed, each times down in seconds after its associated TP input goes away and disallows any new TP service on that input until timed out. Note that the timer is ***programmed in minutes but times down in seconds*** (e.g. 7 min programmed = 420 seconds on the timer screen).

RSVC ALL TIMER: This is global re-service timer, i.e. if programmed, it times down after any TP input goes away and disallows any new TP service until timed out.

TP INPUT EVENT ACTIVITY AND MIST REPORT STATUS SCREEN

This screen can be used to view the current or last registered activity for each TP input 1-6. The last Registered action for each input will remain until a new one replaces it***. Note that this is the same information that is reported to the MIST system***. The difference is that you can only view the last action on the LMD event screen, whereas MIST will store records as they come in for later viewing.

Pg dwn from Fail and Re-service timer screen.....

INPUTS 1-3

#	TIME	ST	C/S/O	PHS	ON	GRN	OFF	EXT
1	10:11:25	3	1/1/1	2/6	75	82	09	0
2	10:43:36	4	1/1/1	4/8	30	30	42	10
3	12:05:50	2	2/1/1	1/6	1	58	40	0

Pg dwn...

INPUTS 4-6

#	TIME	ST	C/S/O	PHS	ON	GRN	OFF	EXT
4	12:56:09	1	1/1/1	2/6	10	0	0	0
5	00:00:00	0	0/0/0	0/0	0	0	0	0
6	00:00:00	0	0/0/0	0/0	0	0	0	0

Say it is now 12:56:15 (TP input 4 is currently active)

The TP input event screen shows the last status of each used input 1-6, where

#: The input number 1-6. Always in order, where input 1 is the first row of the first screen and 6 is the last row of the second screen.

Note: Zero values in a row indicates that the corresponding input *is not used (programmed) or had no activity since the last unit power up. For example, in the example screens above, TP inputs 5 and 6 are either not used or they had no activity of any kind since the last controller power up*

Time: The time of day of the Tpr input event occurrence.

ST: The TP input status as a result of the last event where;

0 = Inactive, not programmed or no activity occurred since last power-up.

1 = TP input has started (is currently active but not in TP phase, not failed, etc.)

2 = TP input was cleared or went away before TP Phases are achieved

3 = TP phases achieved (TP is/was successful)

4 = TP max extend timer timed out before input cleared or went away

5 = Priority override, a higher TP priority input canceled this one

6 = Max Wait Fault. TP max wait timer timed out before TP phases achieved

7 = TP Input failed. The 255 sec. fail timer has timed out and has not returned normal (input stuck on, clears when input goes away).

8 = PE override. TP service canceled due to pre-emption

9 = TP input return normal. Was failed, but returned normal because input went away.

10 = Min re-service refusal. TP service was refused due to min re-service timing

11 = The inhibit (all) input was applied before TP phases achieved

PHS: The ring 1/ring 2 phases active at the time the TP input becomes active. Note that the phase values as set by input activation do not change as a result of any of the other status codes be logged--with the exception of when the input fail timer times out after a max wait time out.

Note: The following ON, GRN and OFF status values represent points in the active cycle. They are meaningful only when the unit is in coordinated operation.

ON: The point in the active cycle that the TP input becomes active

GRN: The point in the active cycle that the TP phase green becomes active. If there is more than one TP phase (dual ring) it is the first point when *both* are green.

OFF: The point in the active cycle that the TP input goes away, clears, or is inhibited due to max wait time out, max extend time out, and/or fail.

RAW TRANSIT PRIORITY INPUTS STATUS SCREEN

Transit priority inputs can also be viewed from the raw inputs screens. To get to these, hit;

Main Menu-1-1-6-8-Page Down 23 times.... .

TPr1X	TPr2	TPr3	TPr4	TPr5	TPr6	TPrI
152X	233	0	0	0	0	0
OR	OR	OR	OR	OR	OR	OR
0	0	0	0	0	0	0

"X's" indicate which input is active. These are the Transit priority call inputs 1-6 and the Transit priority inhibit. See page 2 for input definitions.

Tip: Because of the numerous paging down necessary to get to this screen, it is a good choice for the LMD9200 "Hot Key" function. To use it, simply select the screen using menus and paging down as above. After the screen is obtained, *hit the decimal key then any digit 0-9.* From that point on, the same screen can be selected from any other run screen by pressing that one key 0-9 (do not hit decimal again, that is only for assigning the key the first time).

PG dwn etc. for Transit Priority Call Clear inputs 1-6 and Phase 1-8 conditional transit priority shorten *INHIBIT* inputs.

USE OF TRANSIT PRIORITY FOR QUEUE (BACK-UP) ALLEVIATION

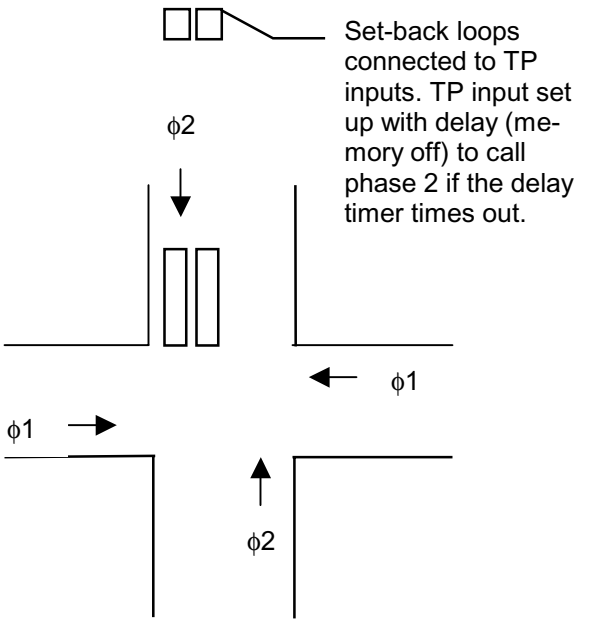
GENERAL

Transit Priority operation was developed to provide more efficient operation for Transit vehicles. During the development process, however, it became apparent that this feature may have other uses as well. Most notably of these is to alleviate queues and temporary back ups at coordinated intersections.

Example

Say that for the coordinated intersection below the Southbound phase 2 approach occasionally overloads and backs-up. Say that when this occurs phase 1 remains fairly normal. Assume that the back-ups are occasional and not continuous. If the back-ups were continuous, the situation would need to be addressed by invoking a longer cycle and/or split with more phase 2 green time for the period.

To address this occasional situation, set-back loops are placed and wired into TP inputs. The TP inputs are set-up with delays and will call phase 2 if the delay timer times out. An appropriate TP extend time is provided.


Set-back loops connected to TP inputs. TP input set up with delay (memory off) to call phase 2 if the delay timer times out.
ϕ2
ϕ1
ϕ1
ϕ2

In some cases such as this, pre-emption may have been used to exhaust the backed-up queue. The TP feature may provide some advantages because, unlike pre-emption, other phases are not as abruptly terminated or skipped and the cycle timing is largely preserved.

SECTION VIII

COMMUNICATIONS SET-UP AND REPORTS

GENERAL

The **COMM SET-UP** section is used to set-up the **LMD** communications and modem ports for the particular application and/or equipment interface.

PROGRAM/READ MENU

```
          --PROGRAM/READ MODE--
1. SECURITY CODE 4. TIME CLOCK  7. REPORTS
2. CONTROLLER    5. PRE-EMPTION
3. COORDINATION  6. COMM SET-UP
```

SELECTION 6…COMM SET-UP

```
           -COMMUNICATIONS SET-UP
1. PRINT/COMM SET-UP    4. SYS MAP PHASES
2. PH #'s & MODEM INIT       (MDM100)
3. SPE  EN  KT MAPPIN 5  TB  BA K-UP DEL
```

PRINTER/SECTION/ADDRESS…..SELECTION 1

```
  --SYSTEM PORT CONNECT TO MASTER--
SYSTEM PORT:  0          SYSTEM # :      1
SYSTEM TYPE: 01          UNIT ADDRESS:   1
--PGDN TO CONTINUE--
```

System Port: Identifies the system communcations port. 0=Modem, 1= RS-232A, or 2= RS-232B.

System Type: Identifies which closed loop system master is being used; 0= LM100 (1200 baud), 1-4 = MIST or CL MATS @ 1200, 2400, 4800, or 9600 BPS.

System # : Master/Zone number (0-99) to which this controller applies if more than one master or zone per comm link (does not apply to LM100).

Address: Local controller address; 1-24 for LM100, 1-30 for MIST, 1-64 for MDM100, 1-64 for CL MATS.

PGDN…

```
       -- NON SYSTEM PORTS SET-UP --
  DIAL MODE:  0      PRINTER PRTY:    3
  COMM MODE: 00      PRINTER BAUD: 1200
  (DIAL-IN)          MONITOR PORT:    2
```

Dial Mode: 0 = Direct RS-232, 1= Hayes compatible modem, 2= UDS modem (most modems today would use the Hayes compatible setting). 3= External 202 type modem (non-dial-up) or **MDM100.**

Comm Mode (i.e. what format): 0 = LM System, 1-4 = CL MATS @ 1200, 2400, 4800, or 9600 BPS

Printer Parity: 0-3, where;

0 = 7 bits no parity
1 = 7 bits odd parity
2 = 7 bits even parity
3 = 7 bits space parity or 8 bits no parity

Note: the printer must be set up for serial operation

Printer Baud Rate: enter the desired baud rate; 300, 1200,2400, 4800,9600 and set printer to the same rate.

Monitor Port: Indicates which RS-232 port to use for interface with LNME series monitors. Use 1 = standard port for *pre-fold down pane!* LMD units *converted to* rev. 5 operation *and* used In the LM system context. Use 2= comm module port for LMD *fold* down *panel* versions (two RS-232 ports). When using fold-down LMD's with direct dial *and* LNME monitor interface, use the standard port for the direct dial and the comm port for the LNME.

PHONE NUMBERS……

```
  --DIRECT DIAL PHONE NUMBERS--     | , W
  PRIMARY: T9W13154576257           | T P
SECONDARY: T9W13156378518           | SPAC
  DP TO SET SPEC FUNC | PGDN FOR DIALER
```

Direct dial phone numbers are related to LMD initiated call-ins using a dial-up modem or direct RS-232 (no system master) . There are 2 telephone numbers—the choice of which telephone is used and when is determined by clock CKT's 114-119 (see clock CKT's, also see reports).

To program the phone numbers;

1. Specify the numbers of the computers to be called at telephone 1 and telephone 2 (set primary and secondary both = 1 for direct RS-232).

2. If special characters are to be used:

-Press the decimal point key at the place you wish to insert the special character.

-Move the pointer with the arrow key until the desired character is selected.

-Press the decimal key once again to insert the character and move to the next digit position.

3. To control the modem speaker, a "T" or "P" must be used as the lead character followed by 0-4 spaces., i.e. the spaces are placed between the "T" or "P" and the

actual number. Spaces used in this way will have the following results;

0 or 1 space	speaker always off
2 spaces	speaker on when dialing only
3 spaces	speaker always off
4 spaces	speaker on during incoming calls only

If no “T” or “P” is used, the speaker will default to off. Special characters provide the following functions:

,	Provides 2 second (default) delay
W	Wait for dial tone
T	Tone (touch tone/pushbutton) type phone
P	Pulse (rotary) type phone
SPAC	Controls speaker when placed immediately after T or P, otherwise no function.

Notes:

1. The T or P should be the lead character when used. Usually for “T” type systems the T can be omitted. “P” must be used for rotary systems.

2. Use “,” (delay) or “W” (wait for dial tone) with phone systems that take a while for the dial tone, particularly for those that require a 7, 8, or 9 first to get a line.
3. Avoid overuse of special characters. Many systems require no special characters at all.

MODEM INIT STRING (PGDN FROM PHONE #’s)…

```
MODEM INIT STRING:

LT/RT AWS MOVE: USE NUM KEYS, UP/DWN AWS
TO SET, END (Y) WITH DP
```

Used to set modem initialization string per modem manufacturer’s recommendations.

SPECIAL FUNCTION CIRCUIT MAPPING

Applies to MDM100 and MIST only. This feature allows the local controller’s time clock circuits to be activated by the MDM100 or MIST. Special function bits 1-32 are issued by the master and are received by the LMD through the system comm port.

PG DWN… For Special functions 9- 24…..

-Circuit specifies which clock ckt function gets activated by the special function bit.

-Delay specifies how long the LMD will wait to activate the specified function after receiving the bit. Delays can vary from intersection to intersection to provide sequenced operation such as route pre-empt below.

Special function circuits could, for example, be used for “route pre-emption” whereby a series of local controllers are pre-empted by the master. By utilizing the time delay feature in varying amounts at each intersection, a sequenced pre-emption can be performed. Intersections within the system that are not associated with the route simply do not have a ckt assigned to the special function bit.

SYSTEM MAP CICUITS (For MDM100 only)

This programming area defines which phases will be displayed on the system wide map at the *Central Office Monitor*. The *System Wide Map Signal Assignments* are sent back to the Central Office Monitor via the MDM100.

From PROGRAM/READ, selection 8…COMM SET-UP…then selection 4….SYS MAP PHASES….

```
 --SYSTEM WIDE MAP SIGNAL ASSIGNMENTS--
SIG1  SIG2  SIG3  SIG4  |   0= NOT USED
  2     4     6     8   | 1-8= PHASES
                        |9-12= O/L A-D
```

TBC BACK-UP DELAY…

```
   --TBC BACK-UP DELAY--
DELAY | 0-255 MINUTES DELAY FROM LAST
      | CARRIER TO TBC BACK-UP
   0 |
```

TBC is the back-up mode for comm interconnect. The back-up delay defines how long the LMD will wait to implement the TBC back-up after carrier (comm) is lost (which may only be brief).

REPORTS

The LMD is capable of logging a number of significant events by time and date. These logs can then be assigned to a specific schedule and, in the direct dial mode automatically called in to Central. Reports can also be uploaded (only) upon request.

FROM PROGRAM/READ…7…REPORTS….

```
            --REPORTS MENU--
1. FUNCTION SCHEDULING    4. CALL DELAY
2. VOLUME LOGGING
3. MOE/SPEED SET-UP
```

SELECTION 1…FUNCTION SCHEDULING

```
      --REPORT FUNCTION SCHEDULING--
FUNCTION UD1 UD2 UD3 UD4 UD5 UD6 UD7 UD8
    MODE   0   0   0   0   0   0   0   0
0=NONE/ 1,2,3=SCHEDULES A,B,C/ 4=REQUEST
```

PG DWN…

```
      --REPORT FUNCTION SCHEDULING--
FUNCTION CLK PWR FRM MMU CHK DET RFL MCE
    MODE   0   0   0   0   0   0   0   0
0=NONE/ 1,2,3=SCHEDULES A,B,C/ 4=REQUEST
```

PG DWN…

```
      --REPORT FUNCTION SCHEDULING--
FUNCTION HPE CYC CRD KEY SYS FLM LPE MOE
    MODE   0   0   0   0   0   0   0   0
0=NONE/ 1,2,3=SCHEDULES A,B,C/ 4=REQUEST
```

Each function is assigned to a schedule. "None" would indicate that the function will not be logged at all. "Request" would indicate that the function will be stored until requested by the PC. Schedules A, B, C are for automatic call-ins. When the LMD9200 is operated in the direct dial mode (no master), schedules A, B, C will automatically call in to the central PC based on time clock circuits 114-119. Each schedule has 2 circuits, one for telephone 1 and another for telephone 2 (see clock CKT's).

In the direct dial mode, the LMD9200 will call in any new data to the indicated telephone (computer) whenever the corresponding circuit is active. Each schedule buffer A,B, and C has a "pointer" for each telephone so that the computer at each telephone receives only data new to it

In the LM100 system, schedules cannot automatically call in but they can be requested and uploaded.

When the LMD200 is used in conjunction with the MDM100, the LMD200 will also call in any new data utilizing one of the first two MDM100 telephone numbers. Corresponding time clock circuits in the MDM100 must be on to allow reporting through the master. Each schedule buffer A, B, and C has a "pointer" for each telephone so that the computer at each telephone receives only data new to it.

Buffer sizes vary as follows:

Schedule Buffer	Size	
A	30	Messages
B	100	Messages
C	100	Messages
Request	60	Messages

The logic behind the buffer sizes is that "A" would be for "priority" messages and would thus have its call-in circuits on all or much of the time. As such, the message log would not build up significantly before calling in. Schedule B and C buffers are larger, intended for once per day or once per week call-ins. Request would be medium sized because only a limited number of functions would likely be assigned to this schedule.

Function Definitions

The following functions are capable of being logged by the LMD. The abbreviations are as they appear on the screen.

Abbreviation	Function
UD1-8	User defined MSD inputs 1-8 The inputs are defined at the PC. A message is logged on ON/OFF transactions of the input. For example, input 1 might indicate "Cabinet door open" at the PC when activated, and "Cabinet door closed" when deactivated. User inputs UD1-5 are AC level, and UD6-8 are DC.
CLK	Real time clock failures.
PWR	Power on/off, power interruption
FRM	Port 1 Faults (framing errors)
MMU	MMU or Monitor status. The status from the MMU via Port 1 or coded status bits from LSM or LNM monitors are interpreted and will be reported as "Conflict", "Red fail", etc.
CHK	Checksum failures (memory failure).
DET	Detector monitor failures and detector return to normal op.
RFL	Enter and exit remote (UCF) flash
MCE	Activation and de-activation of the Manual Control Enable input

(continued)

Function Definitions (cont')

Abbreviation	Function
PRE	Enter/exit Hi priority pre-empt 1-6
CYC	Cycle fail monitor, logged if the controller fails to cycle.
CRD	Coord fail monitor, logged if a phase with a valid call is skipped.
KEY	Keyboard data load. Logs when *any data is loaded* into EEPROM. Only one log registered upon any multiple load sequence with less than 10 min between entries. New log after 10 minutes of no load activity followed by load.
SYS	Enter and exit system operation.
FLM	Flasher monitor. Determines if Flasher AC output CKT's are Functional. Uses MSD AC inputs pin 2 and 5. AC flasher outputs are connected to these inputs. Flasher must drive AC ON/OFF at approx. one Hertz or failure logged. Cannot be used if AC interconnect used (uses offset 1 and 2 inputs).
LPE	Enter/exit Low priority pre-empt 1-6
MOE	MOE log's. See Cycle based MOE's in this section.

LOCAL VOLUME LOGGING

This data is intended for uploads to a PC via the LMSYSTEM, direct dial, or direct to a laptop. To use volume logging, set the sample period for the collection resolution, then select which detectors are to be logged (only selected detectors will be logged). **Volume logging is enabled** by clock circuit 139. Program this circuit to be active during the times of day that logging is desired. **Volume log reporting in the direct dial** mode is enabled by clock ckts 137 (call T1) and 138 (call T2). Activate these to call the data in to the PC (direct dial or MDM100 only).

The **alternate period** is selected by clock circuit 136. Once uploaded to the computer, volume logs can be viewed over any period, so long as that period is longer than the collecting sample period (i.e. 1/2 hour logs can be viewed if the sample period is 30 min or less).

FROM THE REPORTS MENU SELECT VOLUME LOGGING

```
  --LOCAL VOLUME LOG SAMPLING PERIOD--
NORM   0  |1,5,6,10,15,30,60 MINUTES OR
 ALT   0  |0 = DISABLE OR 99 = BY CYCLE
          --PGDN TO CONTINUE--
```

The sampling period determines the period over which each log is collected. The shorter the sampling period, the better the resolution when viewing logs (i.e. you can view smaller time periods), but memory will be used faster. The alternate sampling period **is enabled by clock circuit 136** (old period finishes first). The alternate period might be used at times of day when finer resolution is desired-- say finding the leading or trailing edge of a peak period.

Enter "99" for sample period if it necessary for volume logs to be collected "per cycle" rather than time period.

Also, see CALL-IN DELAY later in this section to prevent a phone call-in (volume log) after each sample period, this will minimize call-ins.

PG DWN....To enable individual detectors

```
--DETECTORS ENABLED FOR VOLUME LOGGING--
  DET    1   2   3   4   5   6   7   8
 MODE   OFF OFF OFF OFF OFF OFF OFF OFF
CHANGES WILL CLEAR VOLUME LOG.  --PGDN--
```

NOTE: If your LMD has insufficient RAM (less than 32K) the display will indicate "INSUFFICIENT RAM" upon selection of the Detectors Enabled screen.

PG DWN...

```
--DETECTORS ENABLED FOR VOLUME LOGGING--
  DET    9  10  11  12  13  14  15  16
 MODE   OFF OFF OFF OFF OFF OFF OFF OFF
CHANGES WILL CLEAR VOLUME LOG.  --PGDN--
```

PG DWN.....DET'S 17-24

--CAUTION--

To maximize storage capacity, memory allocation is a function of the detectors enabled. Thus, re-programming the detectors enabled data will re-configure memory and destroy any existing volume logs in the LMD. Upload volume logs first (before re-programming) if you wish to save any LMD logs currently stored.

Note that LMD volume storage capacity is a function of:

(1) The sampling period; the smaller the samples, the more logs--the more memory is used.

(2) The number of detectors enabled; more enabled--more memory used.

(3) The time logging is enabled (CKT 139); more time--more memory used.

Examples of storage capability are as follows:

# Det's	Sample period	Hrs./Days Collected	# of days Storage
8	5 min	24	3.2
8	5 min	16	4.8
8	15 min	24	9.6
8	15 min	16	14.4
16	5 min	24	1.9
16	5 min	16	2.9
16	15 min	24	5.9
16	15 min	16	8.9
24	5 min	24	1.4
24	5 min	16	2.1
24	15 min	24	4.3
24	15 min	16	6.4

VOLUME LOGGING RUN STATUS SCREEN

Page down from the detectors run status screen, or... hit MAIN MENU--RUN MODE--RUN MODE STATUS--I/O STATUS--DETECTORS (MAIN MENU-1-1-6-7-PGDN-PGDN) to get....

```
DET VOL |# REC'S STORED: T1:   0 T2:  0
DET INP     1       2       3       4
  VOL       0       0       0       0
                   --PGDN TO CONTINUE--
```

PG DWN ETC. through detectors 5-2.

The top row of the display shows the *number of records stored* for both the T1 (telephone 1) and T2 (telephone 2) buffers. The volume counts are *per the sampling period,* i.e. they zero out at the beginning of each new period.

CYCLE BASED MOE'S

MEASURES OF EFFECTIVENESS are time-stamped records of controller performance. The data is collected during whole cycles within a user defined sampling period of 0, 5, 6, 10, 15, 30, or 60 min. An alternate sampling period can be enabled by time of day. Collection is also enabled on a time of day basis so memory will not be used during uninteresting periods. MOE's can be computed during free op as well as in system mode. The LMD can store 400 MOE logs, each consisting of the following;

- Date and time of day of record
- Reason logged (new C/S/O, etc)
- Number of whole cycles
- Active C/S/O, SYS STATUS, Max or max plan in effect
- Volume per phase
- Secs green available per phase
- Secs ave green used per phase
- % phase green utilized
- % phase occupancy during green
- % phase occupancy overall
- Mix of Gap-out's, Force off's, Max-out's per phase
- # of Walk's per phase
- Status of local/sys detectors
- # of high and low priority pre-empts
- True speed for 4 speed traps
- Computed speed (24 detectors)

MOE SET-UP

To collect MOE data, you must; a) program the MOE set-up data and b) turn on clock ckt 141 during periods you wish to collect. Although you may assign MOE's to a function schedule for automatic call-ins (direct mode), it is not necessary to assign them to any schedule for request only. MOE set-up defines the MOE sampling period, speed set-up parameters, and volume/occupancy detector assignment. All other MOE data such as phase volumes, green utilization, occupancy, gap-outs, force off's, etc. need no set-up and will be collected automatically when collection is enabled (ckt 141 on).

Selection 3 from REPORTS menu, MOE/SPEED SET-UP....

```
--LOCAL MOE SET-UP--
NORM   0  | SAMPLE PERIOD IN MINS; USE
 ALT   0  | 0, 5, 6, 10, 15, 30, OR 60
TRAP   0  | DISCARD SPEEDS ABOVE LIMIT
```

NORM = The normal sampling period for each MOE log. Because cycle based MOE's are based on whole cycles, the MOE sample period record will *not actually begin* until the start of the *first* cycle in the period. It will not end until completion of the last cycle *started within* the period. The MOE record can thus run over the end the sample period as it waits until completion of the last cycle. No loss of data occurs because the next record starts at this point.

NOTE: The beginning (or end) of the cycle is defined as the end of the ***ring 1 coordinated phase.*** **This is true in free operation as well as in system (coordinated) operation, so always program at least the ring 1 coord phase.**

ALT = The alternate sampling period, enabled by clock circuit 140. Typically the alternate sampling period would be shorter than the normal period, enabled when finer resolution is desired.

Note: The LMD can store up to 400 MOE records (logs). Shorter sampling periods use up records faster because they occur more often. This should be taken into consideration when setting up sampling periods. Oldest logs are, however, replaced by newest logs when the MOE buffer is full.

TRAP = The upper limit for recorded speed data. Speeds registered over this value are discarded. This parameter has been provided to prevent a few high speed events from skewing the average (there is always the possibility of a few fast vehicles or false measurements registering high speeds--trucks with multiple axles sometimes do this).

SPEED TRAP SET-UP

PG DWN from sampling period screen....

```
SPEED TRAP    A      B      C      D   |0=IN
 DETECTORS  9/10  11/12  13/14  15/16 |1=FT
  DISTANCE    0      0      0      0   |2=CM
     UNITS    0      0      0      0   |3=DCM
```

Speed traps are determined from travel time between pairs of detectors 9-16 (MSD). Each trap consists of two detectors set 10-20 ft apart (any closer is to short to react, any farther is subject to lane switching, multiple vehicles, etc.). Det's 9, 11, 13, and 15 are the lead detectors for their respective traps. Roadway loops should be placed in an area where it unlikely that vehicles would stop or significantly slow down other than due to congestion. For each trap, specify the distance units and the measured distance between roadway loops. The logs will be recorded in MPH if units are inches or feet and KPH if they are centimeters or decimeters. **For best results,** use high quality, fast responding, digital detector amplifiers for speed traps.

COMPUTED SPEED SET-UP

Computed speed is determined from detector occupancies, user calibrated to an equivalent occupancy at 30 MPH (or 30 KPH*). Computed speeds may not be quite as accurate as trap speeds, but have the advantage of allowing use of most standard phase detectors without special modification. This is particularly true because **computed speeds are only stored** when the *phase associated with the detector is green.* This allows use of stop bar detectors without stopped-during-red vehicles skewing the averages. One loop configuration that is unsuitable for speed traps is a long loop, due to the increased likelihood that more than one vehicle will occupy the loop at any one time. About 10-15 ft or so is approaching a range that is too long for a computed speed loop.

*KPH is selected when the speed trap units are set to CM or DCM. Thus, for KPH, set the trap units when using computed speed, even if speed traps are not used.

PG DWN from speed traps set-up screen.....

```
COMP SPEED CALIBRATED AT 30 MPH (50 KPH)
DET INP  1   2   3   4   5   6   7   8
   TIME  0   0   0   0   0   0   0   0
  TIME = 0-255 HUNDREDTHS OF A SECOND
```

PG DWN for detectors 9-16, PG DWN again for 17-24

To set-up computed speed detectors, program the time duration for an average vehicle traveling over that loop at 30 MPH (or 50 KPH). This can be done by using the computed speed run screen and observing vehicles, or by computing the values as follows:

For MPH

Time = 100 x (standard veh length ft+ loop length ft)/44

For KPH

Time = 100 x (stand. veh length m + loop len. m)/13.88

For example, for MPH, say that the standard vehicle length is 18 ft and the loop is 6 ft., then:

Time = 100 x (18 + 6)/44

= 54 hundredths of a second

Load 54 as the time for that loop

MOE VOLUME/OCCUPANCY DETECTOR ASSIGNMENT

One or more detectors may be assigned to a MOE phase for the purpose of collecting volume and occupancy data. If more than one detector is assigned to a phase, the MOE volume and occupancy data will be the sum.

PG DWN.....from COMPUTED SPEED SET-UP

```
   --MOE VOL/OCC DETECTOR ASSIGNMENT--
   DET   1   2   3   4   5   6   7   8
MOE PH   0   0   0   0   0   0   0   0
          --PGDN TO CONTINUE--
```

PG DWN.....for detectors 9-24

INTERPRETATION OF CYCLE BASED MOE'S

An example of an MOE report is shown on page 3D-8. The example is based on an 8 phase dual ring controller, with 2 and 6 as the coordinated phases. All computed speeds are determined from near-stop-bar detectors (within 50 ft of the stop bar), except the speed traps, which are placed mid-block. Following is a description of that report.

HEADING

Title = **First line**: "Local Cycle Based MOE Report"

Second line: System and Intersection name

Reason for Log = The reason the record was closed. In this case it was closed because the sampling period ended. However, records will be closed (and a new one started) if there is any change in the C/S/O/SYS, Max in effect, or flash status within the period. The "Reason for Log" would indicate any of these conditions, as follows:

- End of sample period
- Cycle change
- Split change
- Adaptive split change
- Offset change
- Enter Flash
- Exit Flash
- Enter system
- Enter free
- Max change

Controller type = LMD9200

Sample Period = The *actual* sample period time. Note that this value will most likely *be different* from the programmed sample period. This is because cycle based MOE's are based on *whole cycles*. Based on the timing of the *programmed* period, the *actual* sample starts on the yellow of the first ring 1 coordinated phase of the period, and ends on the yellow of the last coordinated phase *started before* the programmed sample period ends.

Number of cycles = The number of whole cycles. Cycles are referenced to the beginning of yellow of the phase programmed as the ring 1 coordinated phase, both in system and free operation.

Controller status = System (coordinated) or free

Date/Time = The date and time of the record. **Note**: the time is recorded in the *middle* of the sampling period.

Cycle/Split/Offset = The active C/S/O at the time.

Max in Effect = The active Max or Max Plan at the time.

PER PHASE CYCLE BASED MOE DATA

Phase 1-8 = Down the left column indicates phase 1-8

Total volume = The collective volume of all detectors assigned to the phase during the sampling period.

Seconds Green Available Per Cycle = The *green time* allocated to the phase. This is determined in one of two ways, depending on the system (coordination) status:

If in system (coordinated) mode, the green time is determined from the Auto-Calc split percentage values assigned to the active cycle and split in effect. Thus, you must either use auto-calc for calculating force offs and permissives, or you must program in the *equivalent* percentages for your manually calculated force offs. **Note** that the report value green time is automatically calculated and will subtract out yellow and red from the programmed percentage. Thus, the percentage should always include *total phase time*, including yellow and red.

If in free operation (not coordinated), green time is determined from the active max or max plan in effect.

EXAMPLE CYCLE BASED MOE REPORT

Following is an example of an actual LMD Cycle Based MOE report.

Note: When in system mode, green time is assumed to be the Auto-Calc split percentage as indicated above. It does not take into account max's that may be shorter than the split force off. This would, however, be evident if a phase were constantly max'ing out instead of forcing off when in system mode.

Seconds Average Green = The average green time actually used by the phase during the sampling period.

% Average Green Utility = The percentage of green time actually used as a percentage of the allocated green. This is essentially "Seconds Average Green" di-

vided by "Seconds Green Available Per Cycle". This may be one of the more useful indicators in the report. For example, if one phase is using an average of 100% of its allocated green, while another is using only 40%, then it may be an indication that some split time could be taken from the 40% phase and applied to the 100% phase. **Looking at the example**, note that phases 2 and 6 use over 100% of allocated green. *Expect* this to happen on the coordinated phases because early gap-outs of non-coordinated phases often result in an early return to the coordinated phase. The coordinated phase green may then be actually longer than its allocated value.

% Total Occupancy = The sum total % occupancy of all detectors assigned to the phase as a percentage of the *actual* sampling period, regardless of phase indications.

% Green Occupancy = The sum total % occupancy of all detectors assigned to the phase, but tabulated only during green, as a percentage of the actual green time used. Green occupancy may be a *more useful* indicator than total occupancy because it may be *easier to see trends*. Again, in the example, as well as for many of your own applications, the detectors are near-stop bar

Local Cycle Based MOE Report

HENRY CLAY BLVD. and TAFT ROAD

Reason for Log: End of Sample Period
Controller Type: LMD8000 Date: 06/11/92
Sample Period: 16:26 mm:ss Time: 12:08
Number of Cycles: 8 Cycle/Split/Offset: 1 1 1
Controller Status: Free Max in Effect: Max 1

Phase	Total Volume	Seconds Green Available Per Cycle	Seconds Average Green	% Average Green Utility	% Total Occ	% Green Occ	Gap's	F.O.'s	Max's	Walks
1	37	30	11	36	21	19	14	0	1	0
2	100	45	32	71	51	41	7	0	1	0
3	25	40	10	25	38	40	9	0	0	0
4	75	30	30	100	56	36	8	0	0	0
5	65	30	22	73	59	61	8	0	0	0
6	125	45	35	77	57	45	8	0	1	0
7	60	40	14	35	48	45	10	0	1	0
8	90	30	20	66	50	49	7	0	1	0

Comm. Module Installed

Detector	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Ext. Phase	1	2	3	4	5	6	7	8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Failed	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Regular Pre-empts	1	2	3	4	5	6
	0	0	0	0	0	0

Low Priority Pre-empts	1	2	3	4	5	6
	0	0	0	0	0	0

Ave Computed Speed (averaged during green only)

Detector	1	2	3	4	5	6	7	8
Speed	13	22	8	20	12	20	15	20
Detector	9	10	11	12	13	14	15	16
speed	0	0	0	0	0	0	0	0
Detector	17	18	19	20	21	22	23	24
speed	0	0	0	0	0	0	0	0

Ave True Speed

Trap	A	B
Speed	0	0
Trap	C	D
Speed	0	0

LMD CYCLE BASED MOE REPORT

detectors (within 50 lt). As a result, during peak periods, there is likely to be a vehicle waiting on the loop during most or all of the red. This tends to push up total occupancy. For instance, a phase that has 16 seconds green on a 100 second cycle could register up to 84% occupancy—simply due to vehicles waiting for green. *Any further* occupancy during green would be in addition to that. This can make It difficult to see trends. For example, In this same scenario, say the green occupancy changed from 25% to 50%. This Is a doubling of the green occupancy, but the total occupancy would only go from 90 to 94%. This might not appear to be much of a relative change when it in fact it is.

Gap's/F.O.'s/Max's = The mix of-gap-outs, force offs, and max-outs for each phase over the period. The sum of these for a given phase will generally equal the number of cycles—unless the phase was skipped one or more times.

Walks = The number of times the ped was serviced for the given phase (the example intersection does not have peds, thus only 0's are recorded). One use of this parameter is for actuated peds of previously undetermined usage. If it turns out that the ped is seldomly used, consideration may be given to *not including* that ped time in the split, and tolerating an occasional late return to the coord phase.

Comm module installed indicates if the communication module is installed or not.

DETECTOR STATUS

Each detector *1-24* indicates the extend phase it is assigned to (0= the detector is not assigned to extend any phase, typically this would apply to "system" detectors). Also listed is any detector failures, denoted by an 'X' below the phase. A dash Indicates no detector failure, as Is the case for all detectors in the example.

PRE-EMPT STATUS

The number of high and low priority pre-empts occurring during the period is listed for each of the pre-empt sequences. No preempts occurred during the period in the example report. The pre-empt status may be important, not only from the standpoint of determining the frequency of preempts, but may explain unexpected phase data in cases where multiple preempts may have affected traffic flow.

SPEED DATA

The cycle based MOE report provides two types of speed data, computed speed and speed trap speed. The example does not use speed traps, but when used, it is not uncommon for the speed trap speeds to be significantly higher than the computed speeds. This is because the speed traps in most applications are placed mid-block, well away from the stop bar, and not as subject to stops.

MOE STATUS SCREENS

A number of MOE status screens have been provided to view the accumulation of data as well as to aid in setting up MOE parameters. NOTE: MOE status screens may be observed even though clock ckt 141 is not on, i.e. the LMD does not have to be *logging* MOE's. However, a sample period must be programmed, and speed traps and computed speeds do require set-up programming.

From MAIN MENU, Select the RUN MODE submenu....

```
        --BASIC STATUS MENU--
1.RUN MENUS  4.PREEMPT      7.MMU STATUS
2.FAULTS     5.MOE/VOL/STAT 8.TRANSIT PR
3.CLOCK STAT 6.SCHED LOGS
```

SELECTION 5....MOE STATUS

```
            --MOE STATUS MENU--
1. SPEED TRAPS     3. GRN DATA/VOL
2. COMPUTED SPEED  4. MAX S/FO S/GAP'S
                   5. VOL LOG STAT
```

SPEED TRAPS

SELECTION 1 ....SPEED TRAPS....The following run status screen pertains to speed trap information.

```
--SPEED TRAPS; UNITS= MPH--
 TRAP   A    B    C    D  |USE KEYS:
 L SPD   0    0    0    0 |"." = FREEZE
 A SPD   0    0    0    0 |CLR = RELEASE
```

Information on the screen relates to the *current period* as it is computed, where:

L SPD = The last speed trap event registered

A SPD = The average trap speed thus far in the period.

Note: the display can be *frozen* by hitting the decimal key, and *cleared* by the CLR key. The Average speed value will automatically clear at the end of the sample period.

COMPUTED SPEED

SELECTION 2....COMPUTED SPEED. The following run status screen pertains to computed speed information (see page 3E-6 for programming).

```
COMPUTED SPEED; UNITS: MPH, OCC= SEC/100
DET INP  1   2   3   4   5   6   7   8
C SPEED  0   0   0   0   0   0   0   0
OCC      0   0   0   0   0   0   0   0
```

PG DWN FOR DETECTORS 9-16, ETC.

Information on the screen relates to the *current period* as it is computed, where:

C SPEED = The last computed speed value

OCC = The last occupancy in sec/100

Note: The occupancy values can be used to calibrate the detectors (see computed speed programming pg. 3-52)

GREEN DATA/VOLUME

SELECTION 3....GRN DATA/VOL. The following run status screen pertains to green data and volume information.

```
 PHASE    1        2        3        4
AVE GRN   0        0        0        0
GRN UT%   0        0        0        0
   VOL    0        0        0        0
```

PG DWN for phases 4-8.

AVE GRN = The average of actual greens used thus far in the period.

GRN UT %= The average green % utilized thus far in the period (as a percentage of the green allocated).

VOL = The accumulated volume of all detectors assigned to the phase (EXT phase) thus far in the period.

NOTE: All Green/Vol data on the screen will **automatically clear** at the end of the sample period.

MAX'S/F.O.'S/GAPS

SELECTION 4....MAX'S/F.O.'S/GAPS. The following run status screen pertains to green data and volume information. No set-up programming is required.

```
PHASE   1   2   3   4   5   6   7   8
MAX'S   0   0   0   0   0   0   0   0
F.O.'S  0   0   0   0   0   0   0   0
GAP'S   0   0   0   0   0   0   0   0
```

Shows current mix of MAX'S/F.O.'S/ GAPS thus far in the period.

CALL-IN DELAY

Selection 4.....from REPORTS MENU.....

User programmable timers (0-255 minutes) are provided for LMD call-in schedules A, B, C, and volume logs. When an event is logged (stored) the associated timer starts, and then clears upon call-in. The timer continues timing if a new event occurs while timer is already timing. This will enable the schedule to collect a number of events before call-in occurs. Otherwise, it is possible to have a call-in after every volume log (which may have only a one minute sample period) or recorded function. This will limit the amount of call-ins.

```
    CALL-IN DELAY (0-255 MINUTES)
SCHEDULE  A   B   C  VOL
          0   0   0   0
      --  PG DN TO CONTINUE  --
```

USE OF LMD REPORTS

The LMD reports are used in conjunction with the TCT LM system software. This software can be used in the LM closed loop system context or direct dial to the controller.

1. User initiated uploads. In this method the user (at the computer) initiates the call *to the LMD.* This method can be used to upload LMD reports in either the LM closed loop system (LM100 or MDM100) or the LMD direct dial mode.

In the **LM100 system** context, the LMD *does not* automatically call in reports. Thus, all reports and all schedules are on a *request only* basis (upload). As a result, assignment of functions to schedules is more for storage allocation and data segmentation than for scheduling.

In the **direct dial or MDM100** context, the data can be scheduled to automatically call in (*initiated by the LMD* by time of day) as well as upload upon request.

2. Computer set-up. To set up the computer for LMD reports:

a. **COMM TYPE.** In LMCONFIG, set up the LM system software normally for closed loop operation if used in that mode. If the LMD direct dial feature is to be used; set the Com. type to dial-up if phone lines and a modem are used, and set the secondary to FSK. If direct RS232 is used, set the Com. type and secondary as RS-232 .

b. **UPLOAD MODE.** In the LMCONFIG menu, select LMD buff and choose the desired mode you wish your computer to operate in as far as *user initiated* uploading of LMD schedule buffers is concerned;

UPLOAD AND CLR T1
UPLOAD AND CLR T2
UPLOAD T1
UPLOAD T2

Recall that the LMD has two "pointers" for each schedule buffer, one for T1 and one for T2 (telephone 1/2). The pointers allow two separate computers to collect data on separate schedules without redundancy at either. In the LM100 system mode, the LMD *does not call* in to T1 and T2, but the separation can be used to allow two different computers to keep complete records of LMD logs via uploads.

"Upload and clear T1 or T2" (telephone 1/2) would be used at the officially designated "T1" or "T2" computers, indicating that the respective computer will upload the latest schedule log data since the last upload. The T1 or T2 data will *then be cleared* (pointer reset) from the LMD so that only new data will be uploaded the next time without redundancy.

"Upload T1 or T2" would be used for other than the designated record keeping computers. Data new since the last "Upload and clear" will be uploaded, but the T1 or T2 pointers *will not be reset.* This prevents records from being "stolen" from the designated computers. However, successive uploads in this mode would receive redundant data (to avoid this, clear messages *before* uploading).

Note: In the **direct dial** mode, LMD scheduled call-ins *always* reset the appropriate T1 and T2 pointers. Thus, call-ins act as if an "Upload and clear" were executed.

c. Phone Numbers. The procedure differs depending on whether the closed loop system or direct dial is used.

If the closed loop system via the system master is used for uploads, the *intersection phone number* in the controller programming section (last page) **must be** set to a *blank or zero*. In this mode, uploads will take place through the master. Thus, the master phone number would be programmed in the master programming data section. Set the T1 and T2 phones to zero as well, unless you are using both the LM system *and* direct dial calling (you can do both).

If the direct dial method is used, the *intersection phone number* in the controller programming section (last page) **must be programmed with a valid or non-zero phone number** (use a "1" if RS-232). This will inform the LM system software to call directly to the intersection instead of through the master. Program the T1 and T2 phone numbers with the numbers of the two computers *to be called by the LMD.* Set the **COMM TYPE** appropriate for the method used for *LMD initiated* call-ins (this does not affect uploads, see step 1 for COMM TYPE for uploads). Note that T1 and T2 phone numbers as well as COMM type are *checksum* values, i.e.. they **must be downloaded** to the controller. The intersection number never leaves the computer.

d. User defined messages. If any of the LMD MSD inputs are to be used, they must be defined in LMCONFIG under ENTRIES. The inputs each have a text field on the right for transitions to both the active and inactive state. Type in your desired message. For example, "Cabinet Door Open" could be typed in for an input's active state, and "Cabinet Door Closed" for the inactive state. The input would be driven by a refrigerator door type switch. Note that inputs colored in yellow are AC and white are DC.

3. To set the LMD up for direct dial reports:

From the LMD COMM SET-UP menu:

a. Set the **system (1-16) and address (1-60)**. These have to do with file management at the PC. The system determines which "system" the data will be filed under, and the address determines which "intersection".

b. Program the **DIAL MODE** (Hayes or UDS or RS-232)

c. Program the **T1 and T2** telephone numbers (dial-up)

From the LMD Reports menu

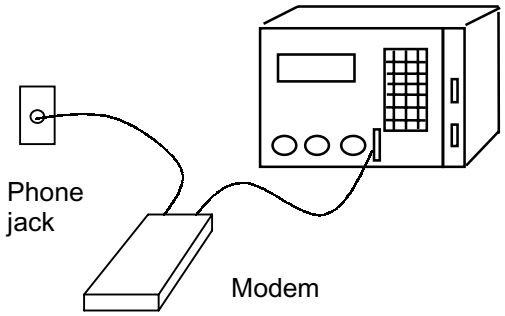
d. Choose **which items are to be logged** by assigning them to a schedule.

From the LMD Detectors menu

e. If detector monitoring is to be used, go to CONTROLLER--DETECTORS/OPTIONS--DETECTORS--DET FAIL MONITOR. Set the sampling time, enable the detectors to be monitored, the phases to be placed on Max Fail Recall upon failure, and the min and max thresholds. **If a phase is to be placed on Max Fail Recall**, then a **MAX Plan 1-8 must be used** (see Serv/Max plans under CONTROLLER-DETECTORS/OPTIONS-SERV/MAXPLANS. Max plans may be implemented by Cycle/Split or CLK CKT's 72-79).

From the LMD Clock menu

f. Set the call in schedule circuits 114-119 appropriately for calling in the indicated schedule A, B, C to the desired phone at the desired time of day. For CKT's to be on full time, set the CKT MODE on for that circuit. For CKT's on/off by TOD, set the CKT MODE AU and program CKT's via day program events.



LMD to modem for direct dial

Each circuit controls a schedule buffer and the phone number to be called. The LMD cannot call in unless one of these circuits Is active. When a circuit is active and a new message occurs, the LMD will call in. Typical use of the circuits would to be to set priorities and schedules. For example, schedule CKT AT1 might be set up to be on all the time(AT1 on = allow schedule A to call in to phone 1). Only priority functions would be assigned to schedule A, thus, any occurrence of such functions would result in immediate call in. Lower priority functions might be assigned to schedule B and/or C which might only call in once per day or week.

T1 vs. T2 can be used to transfer phones by time of day or to separate functions by phone. For example, certain functions could be assigned to schedule A which only calls T1, while others could be assigned to schedule B which only calls T2.

4. Modem set-up The LMD direct call in operation is designed for UDS 212 A/D or Hayes® compatible modems. Most modern modems would use the Hayes compatible setting. Refer to your Peek Sales representative or Distributor for information on preferred modems and proper settings.

The modem Is driven by the LMD RS-232 port, and the modem drives the phone jack. Note that the cable from the LMD to the modem is a special cable (0806147).

SYSTEM OPERATION and LMD REPORTS

Once the LMD and LM system computer software have been set up for reports as previously discussed, the following can be executed;

1. In the direct dial mode, to receive reports via LMD initiated call-ins, the LM system software must be placed in the "monitor mode. If not, and an LMD CKT is active, and new messages are waiting, the LMD will try to call in at intervals as determined by the CALL DELAY setting until successful.

2. To have messages printed as *they arrive,* simply place the printer on line as messages arrive (computer is in LM system monitor mode). To print or view messages after the fact (already uploaded or called in), select the display message log and view or print as desired.

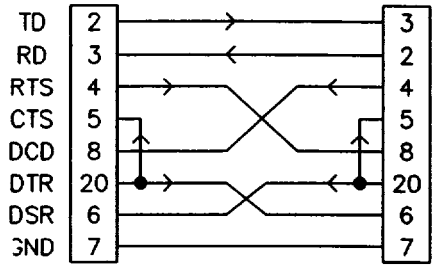
3. In either the LM system or direct dial, reports can be uploaded. To do so, go to the Transfer Menu, Upload From Intersection, and select LMD messages. Upload as desired (see computer set-up, described earlier in this section).

4. In either the LM system or direct dial modes, user initiated calls (to the LMD) can be used for data uploads, downloads, or real time maps.

LNME Conflict Monitor Interface

The LMD can interface, via the RS-232 port, with the LNME conflict monitors (using a TS-1 comm module in TS-1 mode). This feature can be used in either the direct dial or the closed loop system context for remote uploads of conflict monitor message logs, compatibility card information, and switch settings.

A special cable is required for uploading of conflict monitor data. The cable is configured as follows:




```
STATUS:LOGGING LMD SCHEDULE A        SYS:DEANSYS                  08/10/91  12:55:15

08/10/91 12:54  WELLINGTON          IN PRE-EMPTION 1

STATUS:LOGGING LMD SCHEDULE A        SYS:DEANSYS                  08/10/91  12:56:40
08/10/91 12:56  WELLINGTON          OUT OF PRE-EMPTION 1

STATUS:LOGGING LMD SCHEDULE A        SYS:DEANSYS                  08/10/91  12:57:49
08/10/91 12:57  WELLINGTON          DETECTOR  1 CONSTANT CALL
08/10/91 12:57  WELLINGTON          PHASE 1 MAX FAIL RECALL

STATUS:LOGGING LMD SCHEDULE A        SYS:DEANSYS                  08/10/91  12:58:48
08/10/91 12:58  WELLINGTON          DETECTOR  1 RETURN NORMAL
08/10/91 12:58  WELLINGTON          PHASE 1 NORMAL RECALL

STATUS:LOGGING LMD SCHEDULE A        SYS:DEANSYS                  08/10/91  13:06:33
08/10/91 13:06  WELLINGTON          IN CONFLICT

STATUS:LOGGING LMD SCHEDULE A        SYS:DEANSYS                  08/10/91  13:10:04
08/10/91 13:09  WELLINGTON          Cabinet Door Open

STATUS:LOGGING LMD SCHEDULE A        SYS:DEANSYS                  08/10/91  13:11:51
08/10/91 13:11  WELLINGTON          POWER OFF
08/10/91 13:11  WELLINGTON          POWER ON SELF TEST FAILED

STATUS:LOGGING LMD SCHEDULE A        SYS:DEANSYS                  08/10/91  13:12:07
08/10/91 13:11  WELLINGTON          KEYBOARD DATA LOAD

STATUS:LOGGING LMD SCHEDULE A        SYS:DEANSYS                  08/10/91  13:12:43
08/10/91 13:12  WELLINGTON          MAN. CONT. ENABLE ON

STATUS:LOGGING LMD SCHEDULE A        SYS:DEANSYS                  08/10/91  13:15:22
08/10/91 13:14  WELLINGTON          MONITOR RETURN TO NORMAL

STATUS:LOGGING LMD SCHEDULE A        SYS:DEANSYS                  08/10/91  13:16:39
08/10/91 13:16  WELLINGTON          Cabinet Door Closed
```

Sample Message Log

Shown above is an actual message log (slightly reduced) from an LMD which has been set up for direct dial.

SECTION IX

UTILITIES PROGRAM/READ MODE

The Utilities section provides the LMD with file management and other special functions, including:

Back-up plans A variety of "canned" back up plans are provided in PROM. These can be loaded into EEPROM On command.

Clear codes Individually clears functional areas to default values.

Restart Re-initializes controller. Note: A warning is issued upon selection sudden change of indications.

Copy Copies controller programming from one programmed phase to other unprogrammed phase(s).

Diagnostics Internal diagnostics. Refer to TDB 152 for details of diagnostics operation.

Print Allows LMD programmed data to be printed out via serial printer.

Xfer Allows LMD programmed data and real time to be transferred from unit to unit.

Intersection name Alpha-numeric name for print-out

```
          --MAIN MENU--
1.RUN MODE            3.UTILITIES
2.PROGRAM/READ MODE   4.I/O CONFIGURE
     --USE HELP KEY FOR HELP--
```

Selection 3...UTILITIES.....

```
          --UTILITIES--
1.BACKUP/CLR/RESTART/COPY  3.PRINT/XFER
2.INTERSECTION NAME        4.DIAGNOSTICS
```

These are the 4 major categories of Utilities functions. Refer to TDB 161 for use of diagnostics.

Caution: Diagnostics are intended for shop troubleshooting. Diagnostics are not recommended for field use at a live intersection.

BACKUP/CLEAR/RESTART/COPY...Selection 1.

```
    --BACKUP/CLEAR/RESTART/COPY--
1.BACKUP     3.RESTART
2.CLEAR      4.COPY
```

BACKUP...Selection 1..

```
          --BACKUP COPY--
1.CONTROLLER       3.TIME CLOCK
2.COORDINATION
```

CONTROLLER....Selection 1....

```
 --THE CONTROLLER PLAN TO BE USED IS--
1.2 PH S  3.4 PH S  5.6 PH D  7.SPECL
2.3 PH S  4.5 PH D  6.8 PH D
          --END OF SECTION--
```

Select the desired controller back-up code; 2 PH S = 2 phase single ring, 8 PH D = 8 phase dual ring, etc. When selected, the controller will be loaded with timings, sequence, phases used, etc. appropriate for the number of phases and sequence. You may wish to copy the back-up plan then modify to your own needs (which may be a lot easier than starting from scratch).

If one of the choices is selected...

```
      THE BACKUP PLAN IS LOADED

          --END OF SECTION--
```

NOTE: Since the loading of a back-up plan may significantly alter the existing program, **you must re-initialize the controller** before the controller will implement the new plan. This can be done by using the restart command (also under the Utilities menu).

COORDINATION BACK-UP...PRIOR MENU..Selection 2...

```
--THE COORDINATION PLAN TO BE USED IS--
1.2 PH S  3.4 PH S  5.6 PH D
2.3 PH S  4.5 PH D  6.8 PH D
          --END OF SECTION--
```

These are similar to controller back-up plans where 2 PH S = 2 phase single ring, 8 PH D = 8 phase dual ring, etc. In this case however, the data pertains only to coordination parameters; cycle lengths, offsets, force offs, etc.

Also, like the controller data, the screen will prompt you to re-initialize the controller.

TIME CLOCK BACKUP....PRIOR MENU...Selection 3..

```
 --THE TIME CLOCK PLAN TO BE USED IS--
1.TCP1

          --END OF SECTION--
```

There is only one back-up time clock plan at the present time.

NOTE: See Section IV for details on Time Clock, Controller, and Coordination back-up plans.

CLEAR CODES

Back to BACKUP/CLEAR/RESTART/COPY MENU.....

```
    --BACKUP/CLEAR/RESTART/COPY--
1.BACKUP     3.RESTART
2.CLEAR      4.COPY
```

CLEAR...Selection 2....

```
          --CLEAR CODES--
1.CONTROLLER      4.PRE-EMPTION
2.COORDINATION    5.MOES/VOLUMES/SCHEDS
3.TIME CLOCK
```

Used to clear various sections to default values.

Selection 1....CONTROLLER....

```
  WARNING!!!! ALL CONTROLLER DATA
 WILL BE CLEARED TO DEFAULT VALUES
--HIT ENTER IF YOU WISH TO DO SO--
    --PRIOR MENU TO CANCEL--
```

Hit the ENTER key to execute the clear code. Hit PRIOR MENU if you change your mind and do not wish to clear the data. The process is the same for coordination, clock data, and pre-emption. The "MOE/VOLUME/SCHEDULES" clear codes pertain to data collected by the LMD and stored in battery-backed RAM.

RESTART

```
    --BACKUP/CLEAR/RESTART/COPY--
1.BACKUP     3.RESTART
2.CLEAR      4.COPY
```

To restart (re-initialize) the controller....

RESTART.....Selection 3....

```
 WARNING!!!! THE CONTROLLER WILL RE-
INITIALIZE AND SUDDENLY FLASH SIGNALS
   HIT ENTER TO DO SO. BE CAREFUL!!
      --PRIOR MENU TO CANCEL--
```

COPY

```
    --BACKUP/CLEAR/RESTART/COPY--
1.BACKUP     3.RESTART
2.CLEAR      4.COPY
```

To copy controller programming from phase # 1 to all other phases, or to copy controller programming from phase # 1 to all odd phases and phase # 2 to all even phases.....

COPY.....Selection 4....

```
        --COPY FUNCTIONS--
  1.COPY PHASE 2-8 FROM PHASE 1
  2.COPY PHASE 3, 5, 7, FROM PHASE 1
     AND PHASE 4, 6, 8, FROM PHASE 2
```

All controller programming, including; MEMORY, RECALL, CNA, etc., through FWTPCL (flashing walk through ped clearance), all phase timing, including; MIN GREEN through AUTO MAX, SERVICE PLANS, and MAX PLANS will be copied.

INTERSECTION NAME

PRIOR MENU...SELECTION 2.....

```
        --INTERSECTION NAME--    | SEE
NAME: MAIN AND CROSS STREETS     | HELP
USE RT. & LT. ARROWS TO POSITION CURSOR
USE UP AND DN ARROWS TO SELECT CHARACTER
```

The intersection can be named for purposes of identification, file management, printing, etc. Locate the cursor using the left and right arrow keys. Use up and down arrows to scroll through the alpha-numeric characters.

DIAGNOSTICS

The diagnostics routine is defined in TDB 160. Refer to that document, which can be obtained from your distributor or TCT, for diagnostic procedures. **Do note,** however, that the diagnostic routine is **not intended** as a field test procedure. The controller outputs do not function normally. If the diagnostic routine is selected in a field unit, the controller will cycle to all red and will drop CVM (Hi), placing the intersection in flash. Once in the diagnostic routine, the controller **must be restarted** to exit. Both of these requirements are for purposes of intersection safety.

PRINT/DATA TRANSFER

Selection of this menu allows unit to unit data transfer or printout of controller data.

Upon selection of **PRINT/XFER**....

```
          --PRINT/XFER--
1.PRINT            |  NOTE: DATA XFER
2.DATA XFER        |  INITIATED FROM
                   |  DESTINATION UNIT
```

PRINT

The print option requires a printer configured as a **serial printer.** In addition, a special cable (0807252) is required and the LMD **must be set-up** for your printer prior to printout–see Cable Requirements and the Comm Setup menu.

If the LMD is setup for your printer, connect the cable connection with the retaining lock to the LMD RS232 port and the conventional connector to the serial printer. Set the printer paper properly and ready the printer.

Selection 1.....PRINT

```
          --PRINT OPTIONS--
1.CONTROLLER          4.PRE-EMPTION
2.COORDINATION        5.ALL DATA
3.TIME CLOCK
```

Select the desired portion you wish to print out. The print should begin. If the print does not occur, check the RS232 connections, check the LMD Comm Setup, and check the printer. **Note** that instead of printing to a printer, you can also "dump" to a portable computer using a communications software package such as Procomm® and the 0807208(9) cable. Set up an appropriately named "capture file" and act as if the computer is a printer.

DATA XFER

Selection of this option allows keyboard entered data to be transferred from one LMD unit to another.

NOTES:

1. **Initiation** of the data xfer process is from the destination unit, i.e. the unit from which the menu is selected receives the data (from the other unit).

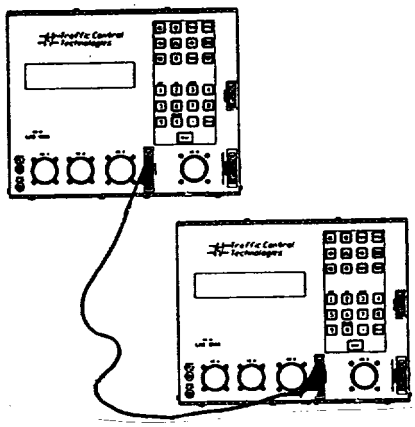
2. **During the transfer** process the data is error checked and stored in a temporary RAM buffer. Only after the entire data segment has been received and checked will the data be transferred to EEPROM and "Working RAM" where it will used by the controller.

3. See the cable requirements section for the proper cable configuration or use TCT cable 0807252.

Selection 2....DATA XFER.....

```
              --DATA XFER--
1.CONTROLLER  3.COORD     5. REAL TIME
2.TIME CLOCK  4.PRE-EMPT  6. ALL DATA
      --DATA XFERS TO THIS UNIT--
```

Connect the cable, one end to each of the two respective LMD units (it doesn't matter which connector goes to which LMD).



Select the desired segment of data. Note that "TIME CLOCK" refers to time clock programmed values such as day program events, week programs, etc. The "REAL TIME" data consists of the actual time of day, date, and year. The "ALL DATA" selection includes the real time data.

After a selection is made, the data begins transferring. While the data transferring the following screen will appear.....

```
DATA XFER IN PROGRESS
  PACKETS RECV'D  "X"
--HIT CLEAR TO CANCEL--
```

The value "X" counts up as packets of data are received. If the data transfers correctly then the screen displays...

"DATA XFERED AND VERIFIED"

This indicates the unit has received data and has Xfered it to EEPROM. If there is a problem, the screen displays....

```
COMMUNICATION FAILURE
DATA XFER CANNOT BE COMPLETED
CHECK CABLE AND/OR CONTROLLER
--HIT PRIOR OR MAIN MENU TO RETURN--
```

No data will have been loaded into EEPROM or working RAM

CABLE REQUIREMENTS FOR PRINT AND DATA XFER

A special cable such as 0807252 is required for both data transfer and print-out for serial printers. This cable is a specially configured NULL cable with 25 pin MALE connectors on both ends. One end of the cable is equipped with a locking retainer and the other is a conventional retainer. **The sliding lock** end must be used on the LMD side when the cable is used for printing. **Either** end may be used on either LMD when used for data xfer.

The 0807252 cable is primarily designed as a data transfer cable–but it will work as a printer cable for many printers. However, there may be printers that would require modifications, such as one with a male or a non-RS232 connector, or one requiring an extra command, etc.

The 0807252 cable is configured as follows:

MALE, SLIDING LOCK SIDE (LMD)			MALE, CONVENTIONAL SIDE (PRINTER/LMD)	
PIN #	FUNC		FUNC	PIN #
2	TXD	——>	RXD	3
3	RXD<	——	TXD	2
5	CTS<	——	SSD	11*
		┌	DSR	6 *
		└	DTR	20*
		┌	CTS	5 *
		└	RTS	4*
7	GND	——	GND	7

NOTE I. Asterisked functions provide for the additional requirements for printer control. The CTS–SSD connection is required for printing if your printer **does not support** "X-ON/X-OFF". The SSD pin normally provides the "READY/ BUSY" signal in most printers. In such cases, the above configuration will work. However, the above configuration **will not** work if your printer **does not** support X-ON/X-OFF, and **does not** use SSD (pin 11) for READY/BUSY. Some printers use DTR or another pin for this function. If so, you must re-wire the cable.

Thus, to print, see if your printer supports X-ON/X-OFF.

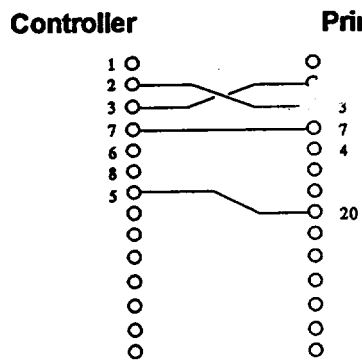
1. If it **does support** X-ON/X-OFF, set it to that mode, and the above configuration should work (see note II).

2. If it **does not support** X-ON/X-OFF, It will still work if the READY/BUSY signal is SSD (pin 11). However, if **READY/BUSY is not pin 11**, the cable must be re-wired such that printer READY/BUSY drives LMD CTS.

NOTE II. Some older printers may require pin 8 (DCD) to be jumpered to pin 20 as well as the pin 20 to pin 6 jumper shown above in the printer connector.

Use of KODAK Diconex® 150 printer

The Kodak Diconex® 150 seems to be an increasingly popular printer. Unfortunately, it does not work with our standard 0807252 cable. To use the Diconex, you can build your own simple cable as shown below:



Recommended Kodak settings:

Panel	Settings	Function
B	All Off	9600 Baud, RDY/BSY protocol
C	1 On	Carrier detect ignored
	2 On	Data set ready ignored
	3 Off	Clear to Send sensed

Recommended LMD settings:

Parity code = 0

Baud rate = 9600

SECTION X

BACK-UP TIMING PLANS

BACK-UP PLANS STORED ON PROM

To minimize programming as much as possible, the LMD contains a set of back-up plans stored on PROM. These can be loaded into the controller upon command from the Utilities Menu. There is a controller and coordination back-up plan for 2, 3, 4, 5, 6, and 8 phase operation. There is also a back-up clock plan. The back-up copy codes, when executed, copy these programs into EEPROM–where they will be used. If the copy codes are not executed, then data that has been loaded through the keyboard will prevail and the back-up data has no effect. Back-up plans may be copied, then modified through the keyboard.

These back-up plans consist of one time clock program, 6 controller, and 6 coordination back-up programs as follows:

TIME CLOCK PROGRAM

2 PHASE CONTROLLER PROGRAM
3 PHASE CONTROLLER PROGRAM
4 PHASE CONTROLLER PROGRAM
5 PHASE CONTROLLER PROGRAM
6 PHASE CONTROLLER PROGRAM
8 PHASE CONTROLLER PROGRAM

2 PHASE COORD PROGRAM
3 PHASE COORD PROGRAM
4 PHASE COORD PROGRAM
5 PHASE COORD PROGRAM
6 PHASE COORD PROGRAM
8 PHASE COORD PROGRAM

Using back-up plans

1. Enter the **Utilities** submenu from the Main Menu, select the back-up option, and follow through for each of desired categories. The data will be transferred from PROM into EEPROM, where it will execute. Once copied, it can be edited as desired.

2. The back-up plan data is listed for each of the plans beginning on page 4-3. Look over the plan appropriate for your application. if the timimgs do not differ significantly from your needs, you may wish to copy the plan into EEPROM then edit. This may prove to be easier than programming entirely from scratch.

Note:

if a **new back-up plan** with a *new* sequence, or a **new sequence** is loaded, a controller restart must be executed (under the Utilities menu) to implement the new plan.

If the **clock is changed** or a **new plan** is loaded, a clock update should be executed. This can be done by going to the PROGRAM/READ MODE --> TIME CLOCK --> UPDATE menu. if not manually executed it will be done automatically ten minutes after the last key stroke. This routine will update the clock to the correct state.

TIME CLOCK BACK-UP PLAN

The LMD also has a back-up time clock plan available as follows. The unit will reflect the indicated plan at the corresponding time of day, day of week, etc.

WEEKDAYS--MONDAY THRU FRIDAY, DAY PROG # 1

From	To	Description
MIDNIGHT	06:00 AM	FREE OPERATION
06:00 AM	07:00 AM	SYSTEM, C1/S1/01
07:00 AM	07:30 AM	C2/S1/01
07:30 AM	08:30 AM	C3/S1/01
08:30 AM	09:00 AM	C2/S2/01
09:00 AM	11:45 AM	C1/S1/02
11:45 AM	13:15 PM	C2/S2/02
13:15 PM	15:00 PM	C1/S1/02
15:00 PM	15:30 PM	C2/S2/03
15:30 PM	17:00 PM	C3/S1/03
17:00 PM	18:00 PM	C4/S1/03
18:00 PM	18:30 PM	C3/S1/03
18:30 PM	19:00 PM	C2/S1/03
19:00 PM	22:00 PM	C1/S1/02
22:00 PM	MIDNIGHT	FREE OPERATION

WEEKENDS--SATURDAY AND SUNDAY, DAY PROG # 2

From	To	Description
MIDNGHT	09:00 AM	FREE OPERATION
09:00 AM	10:00 AM	SYSTEM, C1/S1/02
10:00 AM	19:00 PM	C2/S1/02
19:00 PM	22:00 PM	C1/S1/02
22:00 PM	MIDNIGHT	FREE OPERATION

SPECIAL EXCEPTION DAY--DAY PROGRAM # 3

From	To	Description
MIDNIGHT	09:00 AM	FREE OPERATION
09:00 AM	10:00 AM	SYSTEM, C1/S1/02
10:00 AM	NOON	C3/S3/02
NOON	18:00 PM	C4/S3/02
18:00 PM	20:00 PM	C3/S3/02
20:00 PM	22:00 PM	C1/S1/02
22:00 PM	MIDNIGHT	FREE OPERATION

Exception days Schedule

Exception days are programmed in the back-up time clock plan according to the following schedule:

Except. Day	E. Day #	DP	Type/Description
New Years Day	1	2	Date--Jan 1
Memorial Day	2	2	D/W/M--Last Mon. in May
Fourth of July	3	2	Date--July 4
Labor Day	4	2	D/W/M--1st Mon.in Sept.
Thanksgiving	5	2	D/W/M--4th Thurs in Nov.
Day after Thanks	6	3	D/W/M--4th Fri in Nov.
Christmas Day	7	2	Date--Dec 25
Day after Xmas	8	3	Date--Dec 26

Note: Exception days designated "Date" are of the type that occur on the same date each year, such as Christmas day. Those designated "D/W/M" are of the type that are specific to a day of the week, week of the month, and month of the year, such as Memorial Day, which is the last Monday in May.

The special exception day program # 3 is designed for those heavy shopping days on the day after Thanksgiving and the day after Christmas. The plan provides long mid-day cycles with balanced splits and average offsets.

You may also wish to add exception days assigning this day program to include the *last* Saturday in November and *all* Saturdays in December. This could be accomplished by creating DOW/WOM/MOY exception days for the last Saturday in November (day 7, week 5, month 11) and then for the 1st, 2nd, 3rd, 4th, and 5th (last) Saturday in December. Note that the Saturday after Thanksgiving is always the last Saturday in November and week 5 always represents the last week of the month to the LMD.

Sync Reference Mode

The back-up clock plan uses the "8 independent" type sync reference mode which uses an independent daily reference for each of the cycle lengths. These have been set to reference to Midnight.

The LMD allows 3 other sync reference choices:

Event referencing

End of previous cycle referencing

Absolute referencing (City zero)

Absolute referencing is a non daily reference in which the cycle timers are manually set on a one-time basis and then reference back to this one point in time. There is no daily reference, so the cycle timers will keep in step with a "City Zero" type common reference.

Splits

The back-up plan splits have been set-up so that:

Split 1 = Heavy main
Split 2 = Not as heavy main
Split 3 = Special holiday, heavy all movements including turns
Split 4 = Not used by any of the plans

Offsets

All offsets have been left at zero since offsets generally differ from unit to unit. You must program these on an individual basis in relation to the specific geometry of the system (or from a computer optimization routine, which takes this into account). **Do note**, however, that if you do use the back-up time clock plan, there is an assumption that offset 1 is *inbound* (morning peak), offset 2 is the *average* offset (two way band), and offset 3 is *outbound* (afternoon peak). If the back-up clock plan is used, program the offsets accordingly (see note 2 below).

Coordination Back-up Specifications Chart

The coordination plans are based on the following phasing requirements. In order to effectively use the back-up plans, your application must fit one of the requirements shown. If your application does fit any of these, then you may use the associated back-up plan:

Plan	Ø's Used	Coord Ø's	Sequence
2 phase	1,2	1	Sequential
3 phase	1,2,3	2	Sequential
4 phase	1,2,3,4	2	Sequential
5 phase	1,2,4*,5,6,	2,6	Dual Ring
6 phase	1,2,3,4,5,6	2,6	Dual Ring
8 phase	1-8	2,6	Dual Ring

* If your 5 phase application uses any phase other than phase 4 across the barrier, you could still use the 5 phase back-up, but simply re-program the force offs for the new phase with phase 4's force offs and permissives.

Notes

1. Permissives are set up to allow maximum service to each phase. Permissives for phases the non-coordinated phases start at zero then end an appropriate time before the force off of the associated phase so as to allow service as late as possible without disrupting the return to the coordinated phase.

2. The Coordinated phase has been set up to end (force off) at cycle zero, thus the programmed offsets are referenced to the *end of* the coordinated phase (main street) green. The coodinated phase is Ø1 in the 2 phase plan, and Ø2, or Ø2 and Ø6 in all others.

4. The Coord phases are forced off and may or may not be actuated. If the Coord phase(s) are **not actuated**, place the coord phase(s) on recall max and set the max time appropriate for *free operation.* (i.e. fairly short, say 18-35 seconds). Why set the max for free operation? because during the hours of coordination, the coord phase *will be held* a period longer than the normal max, and will then force off at the correct time. Thus, the shorter time will be in effect only at night (off peak) when the normal max time takes effect. This minimizes long delays at night (off peak) when the main street does not require a long max time. The max time on the coordinated phase essentially has *no effect* on the coordinated phase during coordination.

If the Coord phase(s) **are actuated**, then the coord phase(s) *will still* hold up to the force off point, regardless of coord phase demand--until the first permissive starts. Set the max time on the coord phase as you *usually* would--it will have *no effect* during coordination as it is programmed in the back-up plans.

5. To prevent unwanted max'ing out of the non-corrdinated phases during coordination, you may wish to **call for Max II** during coordination by using the system to automatically call Max II function (internal--no wiring) by following the menu through PROGRAM/READ--COORDINATION--OPTIONS. If you choose to do so, review the previous 2 paragraphs for the coord phase(s) Max II settings. **On non-coordinated** phases, set Max II high enough on each phase so that it will not interfere with the force off points. You may wish instead to use **Inhibit Max** during coordination. In this case, an external wire is required, wrapped from MSD system out (pin 47) to Inhibit Max on the back panel. The system output does not activate until the unit has attained coordination and force offs are being issued.

Max plans can also be used to adjust max times. Max plans can be implemented on a time of day basis or by combination of cycle and split.

BACK-UP PLAN DATA

The back-up plan data from the various back-up plans are shown below.

STANDARD SETTINGS IN ALL PLANS

The settings listed below are common to all the back up plans:

PHASE	1	2	3	4	5	6	7	8
PSG	4	4	4	4	4	4	4	4
WALK	0	0	0	0	0	0	0	0
PCL	0	0	0	0	0	0	0	0
S/A	0	0	0	0	0	0	0	0
TBR	0	0	0	0	0	0	0	0
TTR	0	0	0	0	0	0	0	0
MIN GAP	0	0	0	0	0	0	0	0
MVI	0	0	0	0	0	0	0	0
MAX EXTEND	0	0	0	0	0	0	0	0
AUTO MAX	0	0	0	0	0	0	0	0
AMR	0	0	0	0	0	0	0	0

SECURITY CODE = 1000 (INHIBITED)
MEMORY = ALL OFF
EXT RECALL = ALL OFF
MAX RECALL= ALL OFF
PED RECALL= ALL OFF
CNA I/II = ALL OFF
FL WALK = ALL OFF
SOFT RECALL= OFF
WALK REST= OFF
CONDITIONAL PED= OFF
FLASHING WALK THROUGH PED CLEAR= OFF
INITIALIZE IN 2 (SINGLE) OR 2 AND 6 YELLOW (DUAL)

(continued)

STANDARD SETTINGS IN ALL PLANS (continued)

MINIMUM FLASH = 0
FIRST ALL RED AFTER POWER-UP = 0
OVERLAPS = NONE PROGRAMMED, ALL NORMAL
NO DUAL ENTRY PHASES
NO CONDITIONAL SERVICE PHASES,
SIMULTANEOUS GAP INHIBIT OFF ALL PHASES
RED REVERT = 0 + 2 SECONDS (i.e. 2 SECONDS)
PED ENHANCEMENT = OFF.
FLASHING DON'T WALK THROUGH YELLOW = OFF
INCREASE YELLOW & RED PERCENT = 0%
DET SWITCHING = NONE, STANDARD NEMA
SERVICE PLANS = NONE CALLED, ALL ZERO'S
MAX PLANS = NONE CALLED, ALL ZERO'S

STANDARD COORDINATION DATA IN ALL PLANS

FUNCTION	ENTRY
MANUAL/REMOTE (C,S,O,SYS)	ALL CLOCK MODE
OFFSET SEEKING	SHORTWAY
CYCLES 5-8	ALL ZERO'S
FLOATING FORCE-OFFS	OFF
LOSS SYNC TO FREE	OFF
SYSTEM TO MAX 2	OFF
SYSTEM TO CNA	OFF
PARAMETERS TO FREE	NONE
SUBORDINATED COORD MODE	OFF
COMB TO CALL LEAD/LAG	NONE
ADAPTIVE SPLIT OPERATION	OFF
CSO TO CALL CLOCK CKTS	NONE
COMB TO CALL ALT COORD	NONE

PED PERMISSIVE = 0 (AUTO CALCULATED FROM VEHICLE PERMISSIVES)

FORCE OFF ASSOCIATIONS:

F1 = 1 F5 = 5
F2 = 2 F6 = 6
F3 = 3 F7 = 7
F4 = 4 F8 = 8

PERMISSIVE ASSOCIATIONS:

P1 = 1 P5 = 5
P2 = 2 P6 = 6
P3 = 3 P7 = 7
P4 = 4 P8 = 8

2-8 PHASE BACK UP PLAN DATA

The following data is unique to each of the indicated back-up plans

2 PHASE PLAN

2 PHASE CONTROLLER DATA

PHASE	1	2	3	4	5	6	7	8
MGR	10	8	0	0	0	0	0	0
YELLOW	4.0	4.0	-	-	-	-	-	-
RED	2.0	2.0	0	0	0	0	0	0
MX1	30	30	0	0	0	0	0	0
MX2	30	30	0	0	0	0	0	0

PHASES 1, 2 ON

SEQUENCE = SINGLE RING

2 PHASE COORDINATION DATA

COORD PHASE = 1

CYCLES AND OFFSETS	C1	C2	C3	C4
CYCLE TIMES	45	50	55	60
OFFSETS	--ALL ZERO--			
MAX DWELL	15	15	15	15

2 PHASE FORCE OFFS

	CYC 1				CYC 2			
F.O.	S1	S2	S3	S4	S1	S2	S3	S4
1	0	0	0	0	0	0	0	0
2	18	20	23	25	20	23	25	28
3-8	255	255	255	255	255	255	255	255

	CYC 3				CYC 4			
F.O.	S1	S2	S3	S4	S1	S2	S3	S4
1	0	0	0	0	0	0	0	0
2	22	25	28	30	24	27	30	33
3-8	255	255	255	255	255	255	255	255

2 PHASE PERMISSIVES

CYCLE 1	SPLIT 1		SPLIT 2		SPLIT 3		SPLIT 4	
PERM	ST	E	ST	E	ST	E	ST	E
1	255	255	255	255	255	255	255	255
2	0	4	0	6	0	9	0	11
3-8	255	255	255	255	255	255	255	255

CYCLE 2	SPLIT 1		SPLIT 2		SPLIT 3		SPLIT 4	
PERM	ST	E	ST	E	ST	E	ST	E
1	255	255	255	255	255	255	255	255
2	0	6	0	9	0	11	0	14
3-8	255	255	255	255	255	255	255	255

CYCLE 3	SPLIT 1		SPLIT 2		SPLIT 3		SPLIT 4	
PERM	ST	E	ST	E	ST	E	ST	E
1	255	255	255	255	255	255	255	255
2	0	8	0	11	0	14	0	16
3-8	255	255	255	255	255	255	255	255

CYCLE 4	SPLIT 1		SPLIT 2		SPLIT 3		SPLIT 4	
PERM	ST	E	ST	E	ST	E	ST	E
1	255	255	255	255	255	255	255	255
2	0	10	0	13	0	16	0	19
3-8	255	255	255	255	255	255	255	255

3 PHASE PLAN

3 PHASE CONTROLLER DATA

PHASE	1	2	3	4	5	6	7	8
MGR	8	10	8	0	0	0	0	0
YELLOW	4.0	4.0	4.0	-	-	-	-	-
RED	2.0	2.0	2.0	0	0	0	0	0
MX1	30	30	30	0	0	0	0	0
MX2	30	30	30	0	0	0	0	0

PHASES 1, 2, 3 ON

SEQUENCE = SINGLE RING

3 PHASE COORDINATION DATA

COORD PHASE = 2

CYCLES AND OFFSETS	C1	C2	C3	C4
CYCLE TIMES	70	80	90	100
OFFSETS	--ALL ZERO--			
MAX DWELL	25	25	25	25

3 PHASE FORCE OFFS

	CYC 1				CYC 2			
F.O.	S1	S2	S3	S4	S1	S2	S3	S4
1	38	44	43	42	42	48	48	48
2	0	0	0	0	0	0	0	0
3	21	27	25	21	24	30	28	24
4-8	255	255	255	255	255	255	255	255

	CYC 3				CYC 4			
F.O.	S1	S2	S3	S4	S1	S2	S3	S4
1	47	54	55	54	50	60	60	60
2	0	0	0	0	0	0	0	0
3	27	34	32	27	30	40	35	30
4-8	255	255	255	255	255	255	255	255

3 PHASE PERMISSIVES

CYCLE 1	SPLIT 1		SPLIT 2		SPLIT 3		SPLIT 4	
PERM	ST	E	ST	E	ST	E	ST	E
1	8	24	0	30	0	29	0	28
2	255	255	255	255	255	255	255	255
3	0	7	0	13	0	11	0	7
4-8	255	255	255	255	255	255	255	255

CYCLE 2	SPLIT 1		SPLIT 2		SPLIT 3		SPLIT 4	
PERM	ST	E	ST	E	ST	E	ST	E
1	8	28	0	34	0	34	0	34
2	255	255	255	255	255	255	255	255
3	0	10	0	16	0	14	0	10
4-8	255	255	255	255	255	255	255	255

CYCLE 3	SPLIT 1		SPLIT 2		SPLIT 3		SPLIT 4	
PERM	ST	E	ST	E	ST	E	ST	E
1	8	33	0	40	0	41	0	40
2	255	255	255	255	255	255	255	255
3	0	13	0	20	0	18	0	13
4-8	255	255	255	255	255	255	255	255

CYCLE 4	SPLIT 1		SPLIT 2		SPLIT 3		SPLIT 4	
PERM	ST	E	ST	E	ST	E	ST	E
1	8	36	0	46	0	46	0	46
2	255	255	255	255	255	255	255	255
3	0	16	0	26	0	21	0	16
4 -8	255	255	255	255	255	255	255	255

4 PHASE PLAN

4 PHASE CONTROLLER DATA

PHASE	1	2	3	4	5	6	7	8
MGR	8	10	8	8	0	0	0	0
YELLOW	4.0	4.0	4.0	4.0	-	-	-	-
RED	2.0	2.0	2.0	2.0	0	0	0	0
MX1	30	30	30	30	0	0	0	0
MX2	30	30	30	30	0	0	0	0

PHASES 1, 2, 3, 4 ON

SEQUENCE = SINGLE RING

4 PHASE COORDINATION DATA

COORD PHASE = 2

CYCLES AND OFFSETS	C1	C2	C3	C4
CYCLE TIMES	90	100	110	120
OFFSETS	--ALL ZERO--			
MAX DWELL	30	30	30	30

4 PHASE FORCE OFFS

	CYC 1				CYC 2			
F.O.	S1	S2	S3	S4	S1	S2	S3	S4
1	54	63	64	64	60	70	70	70
2	0	0	0	0	0	0	0	0
3	17	18	22	23	19	20	24	25
4	37	45	45	44	41	50	49	48
5-8	255	255	255	255	255	255	255	255

	CYC 3				CYC 4			
F.O.	S1	S2	S3	S4	S1	S2	S3	S4
1	66	77	77	77	72	84	84	84
2	0	0	0	0	0	0	0	0
3	21	22	26	28	23	24	29	30
4	45	55	54	53	49	60	59	58
5-8	255	255	255	255	255	255	255	255

4 PHASE PERMISSIVES

CYCLE 1	SPLIT 1		SPLIT 2		SPLIT 3		SPLIT 4	
PERM	ST	E	ST	E	ST	E	ST	E
1	0	40	0	49	0	50	0	50
2	255	255	255	255	255	255	255	255
3	0	3	0	4	0	8	0	9
4	0	23	0	31	0	31	0	30
5-8	255	255	255	255	255	255	255	255

CYCLE 2	SPLIT 1		SPLIT 2		SPLIT 3		SPLIT 4	
PERM	ST	E	ST	E	ST	E	ST	E
1	0	46	0	56	0	56	0	56
2	255	255	255	255	255	255	255	255
3	0	5	0	6	0	10	0	11
4	0	27	0	36	0	35	0	34
5-8	255	255	255	255	255	255	255	255

CYCLE 3	SPLIT 1		SPLIT 2		SPLIT 3		SPLIT 4	
PERM	ST	E	ST	E	ST	E	ST	E
1	0	52	0	63	0	63	0	63
2	255	255	255	255	255	255	255	255
3	0	7	0	8	0	12	0	14
4	0	31	0	41	0	40	0	39
5-8	255	255	255	255	255	255	255	255

CYCLE 4	SPLIT 1		SPLIT 2		SPLIT 3		SPLIT 4	
PERM	ST	E	ST	E	ST	E	ST	E
1	0	58	0	70	0	70	0	70
2	255	255	255	255	255	255	255	255
3	0	9	0	10	0	15	0	16
4	0	35	0	46	0	45	0	44
5-8	255	255	255	255	255	255	255	255

5 PHASE PLAN

5 PHASE CONTROLLER DATA

PHASE	1	2	3	4	5	6	7	8
MGR	8	10	0	8	8	10	0	0
YELLOW	4.0	4.0	--	4.0	4.0	4.0	--	--
RED	2.0	2.0	0	2.0	2.0	2.0	0	0
MX1	30	30	0	30	30	30	0	0
MX2	30	30	0	30	30	30	0	0

PHASES 1, 2, 4, 5, 6 ON

SEQUENCE = DUAL RING

5 PHASE COORDINATION DATA

COORD PHASES = 2, 6

CYCLES AND OFFSETS	C1	C2	C3	C4
CYCLE TIMES	70	80	90	100
OFFSETS	--ALL ZERO--			
MAX DWELL	25	25	25	25

5 PHASE FORCE OFFS

	CYC 1				CYC 2			
F.O.	S1	S2	S3	S4	S1	S2	S3	S4
1	38	44	43	42	42	48	48	48
2	0	0	0	0	0	0	0	0
3	255	255	255	255	255	255	255	255
4	21	27	25	21	24	30	28	24
5	38	44	43	42	42	48	48	48
6	0	0	0	0	0	0	0	0
7, 8	255	255	255	255	255	255	255	255

	CYC 3				CYC 4			
F.O.	S1	S2	S3	S4	S1	S2	S3	S4
1	47	54	55	54	50	60	60	60
2	0	0	0	0	0	0	0	0
3	255	255	255	255	255	255	255	255
4	27	34	32	27	30	40	35	30
5	47	54	55	54	50	60	60	60
6	0	0	0	0	0	0	0	0
7 -8	255	255	255	255	255	255	255	255

5 PHASE PERMISSIVES

CYCLE 1	SPLIT 1		SPLIT 2		SPLIT 3		SPLIT 4	
PERM	ST	E	ST	E	ST	E	ST	E
1	8	24	0	30	0	29	0	28
2	255	255	255	255	255	255	255	255
3	255	255	255	255	255	255	255	255
4	0	7	0	13	0	11	0	7
5	8	24	0	30	0	29	0	28
6	255	255	255	255	255	255	255	255
7, 8	255	255	255	255	255	255	255	255

CYCLE 2	SPLIT 1		SPLIT 2		SPLIT 3		SPLIT 4	
PERM	ST	E	ST	E	ST	E	ST	E
1	8	28	0	34	0	34	0	34
2	255	255	255	255	255	255	255	255
3	255	255	255	255	255	255	255	255
4	0	10	0	16	0	14	0	10
5	8	28	0	34	0	34	0	34
6	255	255	255	255	255	255	255	255
7, 8	255	255	255	255	255	255	255	255

CYCLE 3	SPLIT 1		SPLIT 2		SPLIT 3		SPLIT 4	
PERM	ST	E	ST	E	ST	E	ST	E
1	8	33	0	40	0	41	0	40
2	255	255	255	255	255	255	255	255
3	255	255	255	255	255	255	255	255
4	0	13	0	20	0	18	0	13
5	8	33	0	40	0	41	0	40
6	255	255	255	255	255	255	255	255
7, 8	255	255	255	255	255	255	255	255

CYCLE 4	SPLIT 1		SPLIT 2		SPLIT 3		SPLIT 4	
PERM	ST	E	ST	E	ST	E	ST	E
1	8	36	0	46	0	46	0	46
2	255	255	255	255	255	255	255	255
3	255	255	255	255	255	255	255	255
4	0	16	0	26	0	21	0	16
5	0	36	0	46	0	46	0	46
6	255	255	255	255	255	255	255	255
7, 8	255	255	255	255	255	255	255	255

6 PHASE PLAN

6 PHASE CONTROLLER DATA

PHASE	1	2	3	4	5	6	7	8
MGR	8	10	8	8	8	10	0	0
YELLOW	4.0	4.0	4.0	4.0	4.0	4.0	--	--
RED	2.0	2.0	2.0	2.0	2.0	2.0	0	0
MX1	30	30	30	30	30	30	0	0
MX2	30	30	30	30	30	30	0	0

PHASES 1-6 ON

SEQUENCE = DUAL RING

6 PHASE COORDINATION DATA

COORD PHASES = 2, 6

CYCLES AND OFFSETS	C1	C2	C3	C4
CYCLE TIMES	90	100	110	120
OFFSETS	--ALL ZERO--			
MAX DWELL	30	30	30	30

6 PHASE FORCE OFFS

	CYC 1				CYC 2			
F.O.	S1	S2	S3	S4	S1	S2	S3	S4
1	54	63	64	64	60	70	70	70
2	0	0	0	0	0	0	0	0
3	19	22	23	24	20	25	24	24
4	38	44	46	48	40	50	48	48
5	54	63	64	64	60	70	70	70
6	0	0	0	0	0	0	0	0
7, 8	255	255	255	255	255	255	255	255

	CYC 3				CYC 4			
F.O.	S1	S2	S3	S4	S1	S2	S3	S4
1	66	77	78	80	72	84	86	88
2	0	0	0	0	0	0	0	0
3	21	23	26	28	24	26	30	32
4	42	46	52	56	48	52	60	64
5	66	77	78	80	72	84	86	88
6	0	0	0	0	0	0	0	0
7, 8	255	255	255	255	255	255	255	255

6 PHASE PERMISSIVES

CYCLE 1	SPLIT 1		SPLIT 2		SPLIT 3		SPLIT 4	
PERM	ST	E	ST	E	ST	E	ST	E
1	0	40	0	49	0	50	0	50
2	255	255	255	255	255	255	255	255
3	0	3	0	4	0	8	0	9
4	0	23	0	31	0	31	0	30
5	0	40	0	49	0	50	0	50
6	255	255	255	255	255	255	255	255
7, 8	255	255	255	255	255	255	255	255

CYCLE 2	SPLIT 1		SPLIT 2		SPLIT 3		SPLIT 4	
PERM	ST	E	ST	E	ST	E	ST	E
1	0	46	0	56	0	56	0	56
2	255	255	255	255	255	255	255	255
3	0	5	0	6	0	10	0	11
4	0	27	0	36	0	35	0	34
5	0	46	0	56	0	56	0	56
6	255	255	255	255	255	255	255	255
7, 8	255	255	255	255	255	255	255	255

CYCLE 3	SPLIT 1		SPLIT 2		SPLIT 3		SPLIT 4	
PERM	ST	E	ST	E	ST	E	ST	E
1	0	52	0	63	0	63	0	63
2	255	255	255	255	255	255	255	255
3	0	7	0	8	0	12	0	14
4	0	31	0	41	0	40	0	39
5	0	52	0	63	0	63	0	63
6	255	255	255	255	255	255	255	255
7, 8	255	255	255	255	255	255	255	255

CYCLE 4	SPLIT 1		SPLIT 2		SPLIT 3		SPLIT 4	
PERM	ST	E	ST	E	ST	E	ST	E
1	0	58	0	70	0	70	0	70
2	255	255	255	255	255	255	255	255
3	0	9	0	10	0	15	0	16
4	0	35	0	46	0	45	0	44
5	0	58	0	70	0	70	0	70
6	255	255	255	255	255	255	255	255
7, 8	255	255	255	255	255	255	255	255

8 PHASE PLAN

8 PHASE CONTROLLER DATA

PHASE	1	2	3	4	5	6	7	8
MGR	8	10	8	8	8	10	8	8
YELLOW	4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.0
RED	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0
MX1	30	30	30	30	30	30	30	30
MX2	30	30	30	30	30	30	30	30

PHASES 1-8 ON

SEQUENCE = DUAL RING

8 PHASE COORDINATION DATA

COORD PHASES = 2, 6

CYCLES AND OFFSETS	C1	C2	C3	C4
CYCLE TIMES	90	100	110	120
OFFSETS	--ALL ZERO--			
MAX DWELL	30	30	30	30

8 PHASE FORCE OFFS

	CYC 1				CYC 2			
F.O.	S1	S2	S3	S4	S1	S2	S3	S4
1	54	63	64	64	60	70	70	70
2	0	0	0	0	0	0	0	0
3	17	18	22	23	19	20	24	25
4	37	45	45	44	41	50	49	48
5	54	63	64	64	60	70	70	70
6	0	0	0	0	0	0	0	0
7	17	18	22	23	19	20	24	25
8	37	45	45	44	41	50	49	48

	CYC 3				CYC 4			
F.O.	S1	S2	S3	S4	S1	S2	S3	S4
1	66	77	77	77	72	84	84	84
2	0	0	0	0	0	0	0	0
3	21	22	26	28	23	24	29	30
4	45	55	54	53	49	60	59	58
5	66	77	77	77	72	84	84	84
6	0	0	0	0	0	0	0	0
7	21	22	26	28	23	24	29	30
8	45	55	54	53	49	60	59	58

8 PHASE PERMISSIVES

CYCLE 1	SPLIT 1		SPLIT 2		SPLIT 3		SPLIT 4	
PERM	ST	E	ST	E	ST	E	ST	E
1	0	40	0	49	0	50	0	50
2	255	255	255	255	255	255	255	255
3	0	3	0	4	0	8	0	9
4	0	23	0	31	0	31	0	30
5	0	40	0	49	0	50	0	50
6	255	255	255	255	255	255	255	255
7	0	3	0	4	0	8	0	9
8	0	23	0	31	0	31	0	30

CYCLE 2	SPLIT 1		SPLIT 2		SPLIT 3		SPLIT 4	
PERM	ST	E	ST	E	ST	E	ST	E
1	0	46	0	56	0	56	0	56
2	255	255	255	255	255	255	255	255
3	0	5	0	6	0	10	0	11
4	0	27	0	36	0	35	0	34
5	0	46	0	56	0	56	0	56
6	255	255	255	255	255	255	255	255
7	0	5	0	6	0	10	0	11
8	0	27	0	36	0	35	0	34

CYCLE 3	SPLIT 1		SPLIT 2		SPLIT 3		SPLIT 4	
PERM	ST	E	ST	E	ST	E	ST	E
1	0	52	0	63	0	63	0	63
2	255	255	255	255	255	255	255	255
3	0	7	0	8	0	12	0	14
4	0	31	0	41	0	40	0	39
5	0	52	0	63	0	63	0	63
6	255	255	255	255	255	255	255	255
7	0	7	0	8	0	12	0	14
8	0	31	0	41	0	40	0	39

CYCLE 4	SPLIT 1		SPLIT 2		SPLIT 3		SPLIT 4	
PERM	ST	E	ST	E	ST	E	ST	E
1	0	58	0	70	0	70	0	70
2	255	255	255	255	255	255	255	255
3	0	9	0	10	0	15	0	16
4	0	35	0	46	0	45	0	44
5	0	58	0	70	0	70	0	70
6	255	255	255	255	255	255	255	255
7	0	9	0	10	0	15	0	16
8	0	35	0	46	0	45	0	44

SECTION XI

INPUT/OUTPUT

GENERAL

The LMD9000 is available as a type 1 or type 2 version of the TS-2 controller. The LMD9200 (type 2) retains the MSA, B, and C I/O connectors and with this exception, the chassis is the same as the LMD9100 (type 1) series.

Most of the programming and operation are identical, with the exception of I/O run mode screens (which relate to the pin configurations), and a few functions which are not the same.

The following is a brief description of each controller;

Type 1 - The TS-2 type I controller utilizes a 10 pin power connector (MSA) and a minimum of 3 additional ports. Instead of 1 wire for each function, data is sent and received serially via a high speed serial data port (refereed to as the **SDLC, Synchronous Data Link Control or Port 1**). The data exchange takes place between the controller, "Bus Interface Unit(s)" (BIU) on the backpanel, a "Bus Interface Unit" (BIU) on the detector racks(s), and the Malfunction Management Unit (MMU). The MMU will continue monitor signal outputs with individual wire connections.

Type 2 - The TS-2 type 2 controller utilizes TS-1 compatible MSA, MSB, and MSC connectors for conventional interface to the backpanel. In addition to MSA-C, the type 2 controller is also equipped with TS-2 ports 1, 2, and 3 for additional data exchange between the controller, MMU, detector racks, system master, and PC (personal computer).

TS2 type 2 standard for Controllers

The LMD9200 pin configuration and functions have been assigned to meet the NEMA TS2 standard. Thus, all available pins have been assigned in accordance with that standard. The optional "mode" configurations are also based on the TS2 standard.

BIU (Bus Interface Unit)

The BIU provides the communication interface between the controller, the backpanel (terminals and facilities), and the detector racks. Its functions include controlling load switch outputs, the conditioning and conversion of terminal and facilities (i.e., cabinet and police panel switches) and loop detector call inputs for the controller. In effect the BIU converts conventional logic level inputs and outputs to high speed serial communication.

MMU (Malfunction Management Unit)

The MMU uses conventional harnessing for AC signal monitoring, with the addition of a high speed serial port for controller interface. The controller, in constant communication, compares its active phase sequence with the compatibility card programming. Each checks the other and either can place the intersection in flash if there are any discrepancies (the controller flashes the load switches, all red). The SDLC can be disabled for conventional TS-1 compatible monitoring.

TS-2 PORTS

Port 1 - SDLC (Synchronous Data Link Control)

The transfer of data between the controller and peripherals, including terminals and facilities is by means of the SDLC (Synchronous Data Link Control) protocol. This method of data communication was defined by IBM (International Business Machines.

It would easy to think of the SDLC port as a communications network within the cabinet. In this network the controller unit is the supervisor, and the MMU and BIUs are nodes or visible devices on the communication network.

The SDLC port is both "hardware" and "software" defined in the TS-2 standard. Thus, the controller, MMU, and BIU are interchangeable between manufacturers. The SDLC (port 1) can be summarized as follows;

- 15 pin serial interface
- full duplex synchronous communications
- each element (MMU, BIU, detector rack) has a unique address
- handshaking, protocol, CRC are defined by the standard

Port 2 - RS-232C (25 pin)

This port(s) would be used for interface with PCs (personal computers), printers, and external modems. This port is defined in hardware terms only, meaning it would be necessary for the user to have TCT LM-System software installed on a PC to interface with a controller. A SERIAL interface printer would be required for direct-to-controller printing.

Port 3 - System Interface Communications Port (9 pin)

This is a TDM/FSK modem port used for a communications link with remote devices (typically closed loop systems). It is presently hardware defined only; data rates, protocols, data formats, error checking, etc. are left up to the individual manufacturer. For example, in the current TS-2 standard, it is not possible to substitute one manufacturer's controller in another's closed loop system.

Editor's Note: Because of the hardware standard, it would be possible to define a communications software standard. In fact, development is now taking place. At the time of publication, this standard has not yet been defined.

I/O CONFIGURE

PORT 1/BIU/MMU OPTIONS

From MAIN MENU.....

```
          --MAIN MENU--
 1.RUN MODE           3.UTILITIES
 2.PROGRAM/READ MODE  4.I/O CONFIGURE
      --USE HELP KEY FOR HELP
```

Select.....4. I/O CONFIGURE.....

```
        --I/O CONFIGURATION--
1. PORT1/BIU/MMU OPTIONS*
2. CUSTOM I/O MAPPING
3. LOAD I/O CONFIG CHANGES
```

* "NOT USED" will appear if TS-1 comm module

From I/O CONFIGURATION Menu select.....1. PORT 1/BIU/MMU OPTIONS.....

```
     --BIU/PORT 1/MMU OPTIONS--
1. BIU ENABLE        4. GROUP TO CHANNEL
2. PORT 1 OPTIONS
3. PEER ADDRESSES
```

BIU ENABLE

From PORT 1/BIU/MMU OPTIONS Menu select.....1. BIU ENABLE.....

```
T/F BIU   1   2   3   4   5   6   7   8
        OFF OFF OFF OFF OFF OFF OFF OFF
DET BIU   9  10  11  12  13  14  15  16
        OFF OFF OFF OFF OFF OFF OFF OFF
```

The LMD9000, through the SDLC, can communicate with up to 8 T/F (terminals and facilities) BIUs and 8 detector rack BIUs. All utilized BIUs must be enabled if communications is to take place.

PORT 1 OPTIONS

Return to BIU/PORT 1/MMU OPTIONS Menu select..... 2. PORT 1 OPTIONS.....

```
     --PORT 1/BIU/MMU OPTIONS--
1. BIU ENABLE        4. GROUP TO CHANNEL
2. PORT 1 OPTIONS
3. PEER ADDRESSES
```

Select .....2. PORT 1 OPTIONS.....

```
          --PORT 1 OPTIONS
 PEER-TO-PEER POLLING  OFF
          MMU DISABLE  OFF
 TYPE 2 RUN AS TYPE 1  OFF
```

PEER TO PEER POLLING ENABLE

A "PEER TO PEER" network is a network architecture in which each node (visible communication device) has equal communication function and precedence. With this capability in the TS-2 cabinet, it is possible to use the SDLC as a communication channel for external devices. Addresses for these external devices have been set aside for future use. To assign addresses, see PEER ADDRESSES on next page.

MMU DISABLE

In the event a TS-2 Type 2 controller is installed in a TS-1 cabinet, with a TS-1 style conflict monitor, it would be necessary to disable communications to the MMU. A TS-1 conflict monitor would not be equipped with an SDLC (Port 1). It should also be noted that by installing a TS-2 Type 2 controller in a TS-1 cabinet, the controller would default to TS-1 inputs/outputs due to the inactivity of the I/O mode select bits (all I/O mode select bits false

= TS-1 mode). MMU CANNOT be disabled with a TS-2 Type 1 controller.

RUN TYPE 2 AS TYPE 1

Since both Type 1 and 2 controller are equipped with the SDLC, it is possible to install a Type II (with MSA-C) in a Type I cabinet. To do this, the input and outputs to MSA-C must be disabled and communication of inputs and output must be enabled over the SDLC. Select ON for RUN TYPE 2 AS TYPE 1 if this need arises.

PHASE TO LOAD SWITCH

Return to BIU/PORT 1/MMU OPTIONS Menu select..... 3. PHASE TO LOAD SWITCH.....

The association between the phase (signal group) and the load switches (output channels) must be defined at the controller. Continually, the controller is verifying the MMU compatibility programming with its own signal sequence. If an error is detected, the controller (through the MMU) will place the intersection in flash and a latched MMU failure will be the result. Vehicle signals, overlaps, and pedestrian signal must be associated with an MMU channel in the following screens.

```
   --PHASE TO LOAD SWITCH MAPPING--
   (SIGNAL GROUP TO CHANNEL MAPPING)
PHASE     1   2   3   4   5   6   7   8
CHANNEL   1   2   3   4   5   6   7   8
```

PAGE DOWN for OVERLAPS

```
   --PHASE TO LOAD SWITCH MAPPING--
   (SIGNAL GROUP TO CHANNEL MAPPING)
OVERLAP   A   B   C   D
CHANNEL   9  10  11  12
```

PAGE DOWN for PEDESTRIAN SIGNALS

```
   --PHASE TO LOAD SWITCH MAPPING--
   (SIGNAL GROUP TO CHANNEL MAPPING)
PED       1   2   3   4   5   6   7   8
CHANNEL   0  13   0  14   0  15   0  16
```

PEER ADDRESSES

Return to BIU/PORT 1/MMU OPTIONS Menu select..... 4. PEER ADDRESSES.....

See PEER TO PEER POLLING ENABLE, above, for a definition of this function. Enter a number from 0-255 to assign address. Up to 16 external devices can utilize the SDLC for the transmission of data. 0 = no communications on a given channel.

```
   --PEER-TO-PEER POLLING ADDRESSES--
1.      2.      3.      4.      5.
6.      7.      8.      9.     10.
11.    12.     13.     14.     15.     16.
```

CUSTOM I/O MAPPING

From MAIN MENU select.....4. I/O CONFIGURE.....

```
          --MAIN MENU--
 1.RUN MODE            3.UTILITIES
 2.PROGRAM/READ MODE   4.I/O CONFIGURE
     --USE HELP KEY FOR HELP
```

From I/O CONFIGURATION Menu select.....2. CUSTOM I/O MAPPING....

```
        --I/O CONFIGURATION--
1. PORT1/BIU/MMU OPTIONS *
2. CUSTOM I/O MAPPING
3. LOAD I/O CONFIG CHANGES
```

* "(NOT USED)" will be displayed for units equipped will TS-1 comm module.

Upon selection of the CUSTOM I/O MAPPING option the following sub-menu will be displayed.

```
    --INPUT/OUTPUT SPECIAL MAPPING--
         (MAPPING IS DISABLED)
1.TOGGLE MAPPING ENABLE 3.INPUT  MAPPING
2.LOAD A DEFAULT MAP    4.OUTPUT MAPPING
```

Standard TS-2 TYPE II I/O configurations

In the TYPE II version of the LMD9000 controller, eight user selectable (by three mode select pins) MSA, MSB, and MSC connector configurations are defined, in addition to the TS-1 compatible version. These variations, in general, eliminate seldomly used or unassigned (by TS-1) pins and replace them with more current functions such as additional detector inputs, pre-empt, coordination, and/or time clock outputs.

If CUSTOM I/O MAPPING is disabled, which it is by default, the I/O mode is selected by the logic combination

of the three I/O MODE PINS, and the selections on the above screen are disabled. I/O modes are selected by jumpers on the back-panel, low (0 VDC) = ON or active.

If it is necessary that custom I/O be utilized, it will be enabled by selection 1.ENABLE MAPPING, from the above menu, at which time the I/O MODE pins will be disregarded and inputs and outputs will be custom programmed.

The three mode select pins are located on MSA and are labeled I/O mode bit A (pin q), I/O mode B (pin y), and I/O mode bit C (pin HH).

For example, if a cabinet were to be installed in system utilizing FSK communications for closed loop system operation, the back-panel would be wired to provide the MODE 2 (system interface) inputs to the controller.

The combination of the logic level of these pins defines the I/O configuration as follows:

	BIT			
MODE	A	B	C	STATE
0	off	off	off	TS-1
1	on	off	off	Hardwire interconnect
2	off	on	off	System interface
3	on	on	off	Reserved *
4	off	off	on	Reserved *
5	on	off	on	Reserved *
6	off	on	on	Manufacturer specific *
7	on	on	on	Manufacturer specific *

* Presently modes 3-7 disable all I/O mode dependent inputs and outputs.

Mode Dependent Inputs and outputs

There are 24 I/O mode dependent inputs and 24 I/O Mode dependent outputs (see "I/O mode select" pins above). The inputs are the former PHASE HOLD, PHASE OMIT, and PED OMIT. The outputs are the former PHASE CHECK, PHASE NEXT, and PHASE ON. See I/O Pin List for the different modes at the end of this chapter. Mode dependent inputs and outputs are labeled as Mode inputs 1-24 and Mode outputs 1-24, rather than their functions, in the pin list.

NEW (TS-2 Type 2) Inputs

There are also ten "new pins" previously not used on TS-1 controllers, these pins are NOT mode dependent (they are the same for all I/O modes). See Section 2 for descriptions. They are:

I/O mode Select pin (bit) A, B, and C
Call to free *
Test C input
Pre-empt input 3, 4, 5, and 6 *
Indicator Lamp Control

* these inputs are also assigned to MSD pins, if so equipped.

I/O MAPPING

To enable custom mapping select.....1. ENABLE MAPPING.....

```
    --INPUT/OUTPUT SPECIAL MAPPING--
         (MAPPING IS DISABLED)
1.TOGGLE MAPPING ENABLE 3.INPUT  MAPPING
2.LOAD A DEFAULT MAP    4.OUTPUT MAPPING
```

Upon selection of.....1. ENABLE MAPPING the following screen will be displayed.....

```
I/o mapping is enabled now.
 -This means MSA Connector I/o Mode Bits
  are now disabled.
                          -HELP to RET-
```

Followed by.....

```
    --INPUT/OUTPUT SPECIAL MAPPING--
         (MAPPING IS ENABLED)
1.TOGGLE MAPPING ENABLE 3.INPUT  MAPPING
2.LOAD A DEFAULT MAP    4.OUTPUT MAPPING
```

NOTES for CUSTOM MAPPING:

1. Keep in mind, as described earlier, when mapping is DISABLED the function of pins will be defined by I/O mode bits per TS-2.

2. After changing BIU/PORT 1 OPTIONS, LOADING A DEFAULT, CUSTOM PROGRAMMING inputs and outputs, the LOAD I/O CONFIG CHANGES menu selection must be executed. This allows you to finish making all changes before actual implementation. Changes will not be implemented until this selection is executed.

I/O DEFAULT MODES (Back-up plans)

It may be necessary to program inputs and outputs in a manner other than the configurations defined by TS-2. If this is required, it is recommended that a default I/O MAP be first loaded and then edited. The LOAD A DEFAULT I/O MAP feature allows the operator to load and utilize one of the I/O Maps stored in memory. These memory maps can then be edited to a specific application.

RETURN to.....CUSTOM I/O MAPPING menu.....

```
    --CUSTOM INPUT/OUTPUT MAPPING--
         (MAPPING IS DISABLED)
1.ENABLE MAPPING      3.INPUT MAPPING
2.LOAD A DEFAULT MAP  4.OUTPUT MAPPING
```

Select.....2. LOAD A DEFAULT MAP.....

```
    --LOAD A DEFAULT I/O MODE MAP--
0.TYPE2MODE0 3.TYPE2MODE3 6.(NOT USED)
1.TYPE2MODE1 4.TYPE2MODE4 7.(NOT USED)
2.TYPE2MODE2 5.TYPE2MODE5 8.TYPE 1
```

It is possible to configure any and all physical inputs and outputs as any controller function, thereby allowing the controller's seldom used inputs and output (HOLDs, CHECKs and ØONs) to be re-assigned for additional inputs and outputs (e.g., detectors).

Any assignable controller input function can be driven by, up to two, physical inputs (connector pins), on the MS, Communications Inputs (comm module), and/or BIU connectors. Also, any assignable controller output function can be assigned to any physical output (connector pin), on the MS connectors.

Any physical input (connector pin) may drive any number of assignnable input functions. Also, as a standard feature, I/O DEFAULT MAPS are provided so that it is possible to configure all inputs and outputs in one of the standard operating modes without the need to assign each and every function to a physical input or output (connector pin).

For example, it may be necessary to use several USER DEFINED inputs for a particular intersection application. However, say the controller is not equipped with an MSD connector (which usually provides the user-defined inputs). It is possible to utilize unused inputs (pins) for the user-defined inputs.

Virtual Outputs

As the name implies, these are not true "hardware" outputs, but rather assignable outputs that exist only through software programming. These virtual outputs are present if the need arises to drive (activate) an input with an output, without the use of cabinet wiring. There are 24 virtual outputs, numbered from 261 to 284.

Seldom used TS-1pins for functions such as ØON, ØCHECK, ØNEXT, are re-assigned in TS-2 (Type 2) I/O modes 1and 2 (see Mode Dependent Inputs and outputs). It may become necessary to use one or more of these functions to drive an input.

For example, in a particular intersection application it is necessary for a vehicle detector to input a call only when an associated phase is active. Locate the programming screen for vehicle detector # 1 from the INPUT MAPPING selection under the CUSTOM I/O MAPPING Menu (see below). Pin # 129, under VD1 (Vehicle Detector # 1) is MSA pin f. Change the "OR" to an "AND" using the decimal key (.), then also assign any virtual output number below the "AND". We'll use 261 in this case.

Custom Input Mapping Procedure

To enable custom mapping select.....1. TOGGLE MAPPING ENABLE.....

```
    --INPUT/OUTPUT SPECIAL MAPPING--
         (MAPPING IS DISABLED)
1.TOGGLE MAPPING ENABLE 3.INPUT  MAPPING
2.LOAD A DEFAULT MAP    4.OUTPUT MAPPING
```

Upon selection of.....1.ENABLE MAPPING the following screen will be displayed.....

```
I/o mapping is enabled now.
 -This means MSA Connector I/o Mode Bits
  are now disabled.
                              -HELP to RET-
```

Followed by.....

```
    --INPUT/OUTPUT SPECIAL MAPPING--
         (MAPPING IS ENABLED)
1.DISABLE MAPPING    3.INPUT  MAPPING
2.LOAD A DEFAULT MAP 4.OUTPUT MAPPING
```

Select.....3. INPUT MAPPING.....

```
 VD1  VD2  VD3  VD4  VD5  VD6  VD7  VD8
 129  110  213  211  314  316  319  341
 AND   OR   OR   OR   OR   OR   OR   OR
 261    0    0    0    0    0    0    0
```

(above is VD1 programmed per example)

After the the virtual output is assigned to the input, the virtual circuit number (# 261) must also be assigned to the other circuit activating the vehicle detector, in this case "ØON". For this example we'll use phase 1 ON, but any input or output could be used.

Return to.....

```
    --INPUT/OUTPUT SPECIAL MAPPING--
         (MAPPING IS ENABLED)
1.TOGGLE MAPPING ENABLE 3.INPUT  MAPPING
2.LOAD A DEFAULT MAP    4.OUTPUT MAPPING
```

Select.....4. OUTPUT MAPPING.....and PAGE DOWN to.....

```
PHASE    1-8 CHECK/NEXT/ON  OUTPUTS
  0    0    0    0    0    0    0    0
  0    0    0    0    0    0    0    0
 261   0    0    0    0    0    0    0
```

After any I/O configuration changes, you must return to the I/O CONFIGURATION Menu and LOAD I/O CONFIG CHANGES. See this operation later in this section.

PG DWN for remaining functions

Note: Phases 1-8 are represented across top of screen and RED, YELLOW, and GREEN are represented from top to bottom.

Input Programming instructions

To assign a function to a pin or pins, locate the function in the following list to obtain abbreviation. Then, scroll down through INPUT MAPPING screens to locate the associated heading and enter pin number below heading. Up to two pins can be assigned to any input function.

Also see the DEFAULT MAPS list later in this chapter. DEFAULT MAPS for I/O (input/output) configuration are stored in ROM memory to configure the LMD9200 controller in standard TS-2 I/O modes.

"AND"ing, "OR"ing, and "NOT"ing of Inputs

In addition to assigning functions to connector pins, it is also possible to functions to be activated in combinations of other pins or not active when an associated pin is active.

For example, an application may exist where the activation of a particular pre-emption input in combination with certain signal display causes the controller to advance one pre-empt sequence. However, the same activation of that input without the assigned signal display causes the controller to advance to a different pre-empt sequence.

Note pre-empt inputs 1 and 2 on the input programming screen below. They are both activated by the presence of a signal on pin # 440 (this is MSD pin 40, but could be any unused input. See pin list at the end of this chapter). However, along with pin 440, pin 126 must also be active (which happens to be phase 2 green vehicle signal output) to cause the controller to advance to pre-empt sequence # 1. Pre-empt sequence # 2 would be in effect only in the absence of phase 2 green vehicle signal output, indicated by the (-) minus sign (which means "NOT") prior to the entry of pin 126. The end result would be calling one sequence if phase 2 were green and another sequence if it were NOT using the same input.

To toggle between "AND" and "OR" use the decimal point (.) on the keyboard. Likewise, to toggle the minus sign ("NOT") also use the decimal point.

```
PRE1 PRE2 PRE3 PRE4 PRE5 PRE6
 440  440  442  220  221  243
 AND  AND   OR   OR   OR   OR
 126 -126    0  449  434  463
```

Function	Descriptions
VC1-32	Vehicle detectors 1-32
PC1-8	Pedestrian detectors 1-8
HD1-8	Phase hold 1-8
VO1-8	Vehicle phase omit 1-8
PO1-8	Pedestrian phase omit 1-8
PE1-6	Pre-empts 1-6
WRM	Walk rest modifier
MIN	Min recall
SG/CS	Simultaneous gap-out inhibit/ Conditional service
W10	Call to week program 10
ASA-D	Alternate sequence A-D
MCE	Manual control enable
IAD	Interval advance
TSA-C	Test A , B, or C
DIM	Dimming function
LMP	Indicator lamp control
MONA-C	Conflict monitor status bits A-C
MMUF	Malfunction Management Unit flash
LFL	Local flash
FM1-2	Flash monitor 1 & 2
TPA-D	Timing plan A-D
OF1-3	Offset 1-3
CTC	Call to clock
CTF	Call to free
SYN	Sync inhibit
SYS	Call to system
TCS	Time clock sync
INH	Interconnect inhibit
RFL	Remote flash
CNA1-2	Call to non-actuated 1-2
FO1-2	Force-off ring 1 & 2
IM1-2	Inhibit MAX timing ring 1 & 2
OR1-2	Omit red clearance ring 1 & 2
PR1-2	Pedestrian re-cycle ring 1 & 2
RR1-2	Red rest ring 1 & 2
ST1-2	Stop time ring 1 & 2
UD1-8	User defined 1-8
AD0-7	Address bits 0-7
VC33-64	Vehicle detectors 33-64

Custom Output Mapping Procedure

To assign a function to a pin, scroll down through OUTPUT MAP screens to locate the heading and enter pin number below heading. Only one pin may be assigned to each output.

Also see the I/O DEFAULT MODES. Back-up plans (DEFAULT MODES) for I/O (input/output) mapping are stored in ROM memory to configure the LMD9200 controller in standard TS-2 modes.

NOTES for CUSTOM MAPPING:

1. Keep in mind, as described earlier, when mapping is DISABLED the function of pins will be defined by I/O mode bits per TS-2.

2. After changing BIU/PORT 1 OPTIONS, LOADING A DEFAULT, CUSTOM PROGRAMMING inputs and outputs, the LOAD I/O CONFIG CHANGES menu selection must be executed. This allows you to finish making all changes before actual implementation. Changes will not be implemented until this selection is executed.

Function	Descriptions
Phase 1-8	Red/yellow/green drivers
Overlap	Red/yellow/green drivers
Ped 1-8	Don't walk/ped clear/walk outputs
Phase 1-8	Check/next/on outputs
PLNA-D	Timing plan A-D
OFF1-3	Offset 1-3
AUX1-4	Auxiliary time clock circuits
SYS	System out
SYSC	Call to system
PE1-6	Pre-empts 1-6
FL	Flash out
FLO	Flashing logic out
CSA-C1	Coded status bit A-C ring 1
CSA-C2	Coded status bit A-C ring 2
FFL	Fast flash status
FFLO	Fast flash logic
ADW1-8	Advanced warning 1-8
ADWA-D	Advanced warning A-D
SF1-24	Special function bit 1-24
DS1-16	Detector simulator outputs 1-16

From MAIN MENU select.....4. I/O CONFIGURE.....

```
          --MAIN MENU--
1.RUN MODE            3.UTILITIES
2.PROGRAM/READ MODE   4.I/O CONFIGURE
     --USE HELP KEY FOR HELP
```

From I/O CONFIGURATION Menu select.....2. CUSTOM I/O MAPPING....

```
          --I/O CONFIGURATION--
1. PORT1/BIU/MMU OPTIONS
2. CUSTOM I/O MAPPING
3. LOAD I/O CONFIG CHANGES
```

Upon selection of the CUSTOM I/O MAPPING option the following sub-menu will be displayed.

```
    --INPUT/OUTPUT SPECIAL MAPPING--
         (MAPPING ID ENABLED)
1.TOGGLE MAPPING ENABLE 3.INPUT  MAPPING
2.LOAD A DEFAULT MAP    4.OUTPUT MAPPING
```

Selection 4.....**OUTPUT MAPPING**

```
PHASE    1-8 RED/YELLOW/GREEN  OUTPUTS
 104  106  206  207  308  307  306  304
 123  125  205  226  309  331  305  328
 140  126  204  225  332  330  329  345
```

PG DWN for remaining functions

Note: Phases 1-8 are represented across top of screen and RED, YELLOW, and GREEN are represented form top to bottom.

PHASE OUTPUTS determine which load switch outputs correspond to the indicated signal.

LOADING I/O CONFIGURATION CHANGES

After changing BIU/PORT 1 OPTIONS, LOADING A DEFAULT, CUSTOM PROGRAMMING inputs and outputs, the LOAD I/O CONFIG CHANGES menu selection must be executed. This allows you to finish making all changes before actual implementation. Changes will not be implemented until this selection is executed.

Return to..... I/O CONFIGURATION Menu.....
select 3. LOADING I/O CONFIGURATION CHANGES

```
          --I/O CONFIGURATION--
1. PORT1/BIU/MMU OPTIONS
2. CUSTOM I/O MAPPING
3. LOAD I/O CONFIG CHANGES
```

When selected….the following screen will be displayed

```
 WARNING! THE CONTROLLER WILL REMAP
 ALL INPUTS AND OUTPUTS TO RFLECT
 ANY CHANGES MADE.   BE CAREFUL
--ENTER TO REMAP—PRIOR MENU TO CANCEL--
```

As the above screen indicates, any and all I/O configuration changes will be implemented, including signal outputs. USE CAUTION when doing so in the field.

If ENTER is pressed, the following screen will be displayed to indicate the changes have been made.

```
    --I/O CONFIG CHANGES LOADED—

                          -PRIOR MENU-
```

Hit PRIOR MENU to return to the I/O Configuration menu.

PIN-OUTS

Pin-outs are defined in terms of the TS2 I/O mode select bits A B and C.

TS2 mode configurations are selected by TS2 type 2 I/O mode bit input pins A, B, C as follows;

I/O mode Input A = A-q
I/O mode Input B = A-y
I/O mode Input C = A-HH

Selection State table Inputs are DC gnd = ON

Mode	A	B	C	State
0	Off	Off	Off	TS1 Mode
1	On	Off	Off	TS2 Hardwire Inter.
2	Off	On	Off	TS2 System

An asterisk under Mode indicates that the fucntion is not mode dependent and does not change from mode mode to mode.

NOTE: Only modes 0-2 are defined in the LMD. Modes 4-7 are future and are not defined at this time.

MS Connector A LMD09200 Pin Termination Assignments:

			MODE FUNCTIONS		
PIN #	**LMD9200 FUNCTION**	**I/O REF NUMBER**	**MODE 0**	**MODE 1**	**MODE 2**
A	Fault Monitor	101	*	*	*
B	24 VDC	102	*	*	*
C	Voltage Monitor	103	*	*	*
D	Ph 1 Red	104	*	*	*
E	Ph 1 Dont Walk	105	*	*	*
F	Ph 2 Red	106	*	*	*
G	Ph 2 Dont Walk	107	*	*	*
H	Ph 2 Ped Clear	108	*	*	*
J	Ph 2 WALK	109	*	*	*
K	Ph 2 veh call	110	*	*	*
L	Ph 2 ped call	111	*	*	*
M	Mode input 2	112	Ph 2 hold	Preempt 3 in	Preempt 3 in
N	Stop time (1)	113	*	*	*
P	Inhibit Max R1	114	*	*	*
R	Ext Start	115	*	*	*
S	Int advance	116	*	*	*
T	Ind. lamp control	117	N/U	*	*
U	AC-	118	*	*	*
V	Earth ground	119	*	*	*
W	Logic ground	120	*	*	*
X	Flashing Logic	121	*	*	*
Y	Status bit C	122	*	*	*
Z	Ph 1 Yellow	123	*	*	*
a	Ph 1 Ped Clear	124	*	*	*
b	Ph 2 Yellow	125	*	*	*
c	Ph 2 Green	126	*	*	*
d	Mode output 18	127	Ph 2 check	AutoFlash	AutoFlash
e	Mode output 2	128	Ph 2 phase on	Preempt 3 out	Preempt 3 out
f	Ph 1 veh call	129	*	*	*
g	Ph 1 ped call	130	*	*	*
h	Mode input 1	131	Ph 1 hold	Preempt 1 in	Preempt 1 in
i	Force off (1)	132	*	*	*
j	Ext Min recall	133	*	*	*
k	MCE	134	*	*	*
m	CNA I	135	*	*	*
n	Test A	136	*	*	*
p	AC+	137	*	*	*
q	I/O mode bit A	138	*	*	*

MS Connector A LMD9200 Pin Termination Assignments (continued):

			MODE FUNCTIONS		
PIN #	**LMD9200 FUNCTION**	**I/O REF NUMBER**	**MODE 0**	**MODE 1**	**MODE 2**
r	Status bit B (R1)	139	*	*	*
s	Ph 1 Green	140	*	*	*
t	Ph 1 Walk	141	*	*	*
u	Mode output 17	142	Ph 1 check	System out	System out
v	Mode input 18	143	Ph 2 ped omit	Auto flash	Local flash
w	Omit red clear R1	144	*	*	*
x	Red rest mode R1	145	*	*	*
y	I/O mode bit B	146	*	*	*
z	CNA II	147	*	*	*
AA	Test B	148	*	*	*
BB	Walk rest modifer	149	*	*	*
CC	Status bit A	150	*	*	*
DD	Mode output 1	151	Ph 1 phase on	Preempt 1out	Preempt 1 out
EE	Mode input 17	152	Ph 1 ped omit	Dim input	Dim input
FF	Ped recycle R1	153	*	*	*
GG	Max II select	154	*	*	*
HH	I/O mode bit C	155	*	*	*

MS Connector B LMD9200 Pin Termination Assignments:

			MODE FUNCTIONS		
PIN #	**LMD9200 FUNCTION**	**I/O REF NUMBER**	**MODE 0**	**MODE 1**	**MODE 2**
A	Mode output 9	201	Ph 1 phase next	Preempt 2 out	Preempt 2 out
B	Pre-empt 2 input	202	N/U	*	*
C	Mode output 10	203	Ph 2 phase next	Preempt 4 out	Preempt 4 out
D	Ph 3 Green	204	*	*	*
E	Ph 3 Yellow	205	*	*	*
F	Ph 3 Red	206	*	*	*
G	Ph 4 Red	207	*	*	*
H	Ph 4 Ped Clear	208	*	*	*
J	Ph 4 Dont Walk	209	*	*	*
K	Mode output 20	210	Ph 4 check	N/U	N/U
L	Ph 4 veh call	211	*	*	*
M	Ph 4 ped call	212	*	*	*
N	Ph 3 veh call	213	*	*	*
P	Ph 3 ped call	214	*	*	*
R	Mode input 11	215	Ph 3 omit	Time plan C	Veh det 17
S	Mode input 10	216	Ph 2 omit	Veh det 12	Veh det 12
T	Mode input 21	217	Ph 5 ped omit	Offset1	Address 2
U	Mode input 9	218	Ph 1 omit	Veh det 11	Veh det 11
V	Ped recycle R2	219	*	*	*
W	Pre-empt 4 input	220	N/U	*	*
X	Pre-empt 5 input	221	N/U	*	*
Y	Ph 3 Walk	222	*	*	*
Z	Ph 3 Ped Clear	223	*	*	*
a	Ph 3 Dont Walk	224	*	*	*
b	Ph 4 Green	225	*	*	*
c	Ph 4 Yellow	226	*	*	*
d	Ph 4 Walk	227	*	*	*
e	Mode output 4	228	Ph 4 phase on	TBC Aux 2 out	TBC Aux 2 out
f	Mode output 12	229	Ph 4 phase next	Preempt 6 out	Preempt 6 out
g	Mode input 12	230	Ph 4 omit	Time plan D	Veh det 18
h	Mode input 4	231	Ph 4 hold	Veh det 10	Veh det 10
i	Mode input 3	232	Ph 3 hold	Veh det 9	Veh det 9
j	Mode input 19	233	Ph 3 ped omit	Time plan A	Address 0
k	Mode input 22	234	Ph 6 ped omit	Off 2 in	Addr 3
m	Mode input 23	235	Ph 7 ped omit	Off 3 in	Addr 4
n	Mode input 24	236	Ph 8 ped omit	TBC online	MMU flash
p	O/L A Yellow	237	*	*	*
q	O/L A Red	238	*	*	*

MS Connector B LMD9200 Pin Termination Assignments (continued):

			MODE FUNCTIONS		
PIN #	**LMD9200 FUNCTION**	**I/O REF NUMBER**	**MODE 0**	**MODE 1**	**MODE 2**
r	Mode output 19	239	Ph 3 check	TBC Aux 3 out	TBC Aux 3 out
s	Mode output 3	240	Ph 3 phase on	TBC Aux 1 out	TBC Aux 1 out
t	Mode output 11	241	Ph 3 phase next	Preempt 5 out	Preempt 5 out
u	O/L D Red	242	*	*	*
v	Pre-empt 6 input	243	N/U	*	*
w	O/L D Green	244	*	*	*
x	Mode input 20	245	Ph 4 ped omit	Time plan B	Address 1
y	Free	246	N/U	*	*
z	Max II select R2	247	*	*	*
AA	O/L A Green	248	*	*	*
BB	O/L B Yellow	249	*	*	*
CC	O/L B Red	250	*	*	*
DD	O/L C Red	251	*	*	*
EE	O/L D Yellow	252	*	*	*
FF	O/L C Green	253	*	*	*
GG	O/L B Green	254	*	*	*
HH	O/I C Yellow	255	*	*	*

MS Connector C LMD9200 Pin Termination Assignments:

PIN #	LMD9200 FUNCTION	I/O REF NUMBER	MODE FUNCTIONS MODE 0	MODE 1	MODE 2
A	Status bit A (R2)	301	*	*	*
B	Status bit B (R2)	302	*	*	*
C	Ph 8 Dont Walk	303	*	*	*
D	Ph 8 Red	304	*	*	*
E	Ph 7 Yellow	305	*	*	*
F	Ph 7 Red	306	*	*	*
G	Ph 6 Red	307	*	*	*
H	Ph 5 Red	308	*	*	*
J	Ph 5 Yellow	309	*	*	*
K	Ph 5 Ped Clear	310	*	*	*
L	Ph 5 Dont Walk	311	*	*	*
M	Mode output 13	312	Ph 5 phase next	Offset 3 out	Offset 3 out
N	Mode output 5	313	Ph 5 phase on	TimePlan A out	TimePlan A out
P	Ph 5 veh call	314	*	*	*
R	Ph 5 ped call	315	*	*	*
S	Ph 6 veh call	316	*	*	*
T	Ph 6 ped call	317	*	*	*
U	Ph 7 ped call	318	*	*	*
V	Ph 7 veh call	319	*	*	*
W	Ph 8 ped call	320	*	*	*
X	Mode input 8	321	Ph 8 hold	Veh det 16	Veh det 16
Y	Force off R2	322	*	*	*
Z	Stop Time R2	323	*	*	*
a	Inhibit Max R2	324	*	*	*
b	Test C	325	N/U	*	*
c	Status bit C (R2)	326	*	*	*
d	Ph 8 Walk	327	*	*	*
e	Ph 8 Yellow	328	*	*	*
f	Ph 7 Green	329	*	*	*
g	Ph 6 Green	330	*	*	*
h	Ph 6 Yellow	331	*	*	*
i	Ph 5 Green	332	*	*	*
j	Ph 5 Walk	333	*	*	*
k	Mode output 21	334	Ph 5 check	N/U	SysSpecFunc 1
m	Mode input 5	335	Ph 5 hold	Veh det 13	Veh det 13
n	Mode input 13	336	Ph 5 omit	Alt seq A	Veh det 19
p	Mode input 6	337	Ph 6 hold	Veh det 14	Veh det 14
q	Mode input 14	338	Ph 6 omit	Alt seq B	Veh det 20

MS Connector C LMD9200 Pin Termination Assignments (continued):

			MODE FUNCTIONS		
PIN #	**LMD9200 FUNCTION**	**I/O REF NUMBER**	**MODE 0**	**MODE 1**	**MODE 2**
r	Mode input 15	339	Ph 7 omit	Alt seq C	UD1
s	Mode input 16	340	Ph 8 omit	Alt seq D	UD2
t	Ph 8 veh call	341	*	*	*
u	Red rest R2	342	*	*	*
v	Omit red clear R2	343	*	*	*
w	Ph 8 Ped Clear	344	*	*	*
x	Ph 8 Green	345	*	*	*
y	Ph 7 Dont Walk	346	*	*	*
z	Ph 6 Dont Walk	347	*	*	*
AA	Ph 6 Ped Clear	348	*	*	*
BB	Mode output 22	349	Ph 6 check	N/U	SysSpecFunc 2
CC	Mode output 6	350	Ph 6 phase on	TimePlan B out	TimePlan C out
DD	Mode output 14	351	Ph 6 phase next	TimePlan C out	TimePlan C out
EE	Mode input 7	352	Ph 7 hold	Veh det 15	Veh det 15
FF	Mode output 24	353	Ph 8 check	N/U	SysSpecFunc 4
GG	Mode output 8	354	Ph 8 phase on	Offset 2 out	Offset 2 out
HH	Mode output 16	355	Ph 8 phase next	N/U	N/U
JJ	Ph 7 Walk	356	*	*	*
KK	Ph 7 Ped Clear	357	*	*	*
LL	Ph 6 Walk	358	*	*	*
MM	Mode output 23	359	Ph 7 check	N/U	SysSpecFunc 3
NN	Mode output 7	360	Ph 7 phase on	Offset 1 out	Offset 1 out
PP	Mode output 15	361	Ph 7 phase next	TimePlan D out	TimePlan D out

MS Connector D LMD9200 Pin Termination Assignments:

PIN #	LMD9200 FUNCTION	I/O REF NUMBER	MODE FUNCTIONS MODE 0	MODE 1	MODE 2
1	Flash	401	*	*	*
2	Offset 1	402	*	*	*
3	Interconnect com	403	*	*	*
4	User defined in 6	404	*	*	*
5	Offset 2	405	*	*	*
6	Offset 3	406	*	*	*
7	Time plan A	407	*	*	*
8	User defined in 7	408	*	*	*
9	User defined in 8	409	*	*	*
10	Call to free	410	*	*	*
11	Call to week 10	411	*	*	*
12	Time plan B	412	*	*	*
13	Time plan C	413	*	*	*
14	Time plan D	414	*	*	*
15	Alt seq A	415	*	*	*
16	Alt seq B	416	*	*	*
17	Alt seq C	417	*	*	*
18	Dimming	418	*	*	*
19	Monitor status C	419	*	*	*
20	System input	420	*	*	*
21	Alt seq D	421	*	*	*
22	Monitor status A	422	*	*	*
23	Monitor status B	423	*	*	*
24	Veh det 13	424	*	*	*
25	Veh det 9	425	*	*	*
26	Veh det 10	426	*	*	*
27	Veh det 11	427	*	*	*
28	Polarizing pin				
29	Veh det 12	429	*	*	*
30	Veh det 14	430	*	*	*
31	Veh det 15	431	*	*	*
32	Veh det 16	432	*	*	*
33	SGO/Cond. serv.	433	*	*	*
34	Pre-empt in 5	434	*	*	*
35	Pre-empt out 1	435	*	N/U	N/U
36	Pre-empt out 2	436	*	N/U	N/U
37	Interconnect inh.	437	*	*	*
38	Time clock sync	438	*	*	*

MS Connector D LMD9200 Pin Termination Assignments (continued):

PIN #	LMD9200 FUNCTION	I/O REF NUMBER	MODE FUNCTIONS MODE 0	MODE 1	MODE 2
39	Sync inhibit	439	*	*	*
40	Pre-empt in 1	440	*	*	*
41	Pre-empt in 2	441	*	*	*
42	Pre-empt in 3	442	*	*	*
43	Pre-empt out 3	443	*	N/U	N/U
44	Polarizing pin				
45	Pre-empt 4 out	445	*	N/U	N/U
46	Pre-empt 5 out	446	*	N/U	N/U
47	System out	447	*	*	*
48	Pre-empt 6 out	448	*	*	*
49	Pre-empt in 4	449	*	*	*
50	Clock ckt 9(Aux 1)	450	*	N/U	N/U
51	Clock ckt 10(aux 2)	451	*	N/U	N/U
52	Clock ckt 11(aux 3)	452	*	N/U	N/U
53	Clock ckt 12(aux 4)	453	*	N/U	N/U
54	Clock ckt 13(sys)	454	*	*	*
55	Clock ckt 8(flash)	455	*	*	*
56	Clock ckt 3(off. 1)	456	*	N/U	N/U
57	Clock ckt 4(off.2)	457	*	N/U	N/U
58	Clock ckt 5(off.3)	458	*	N/U	N/U
59	Clock ckt 1(T/P A)	459	*	N/U	N/U
60	Clock ckt 2(T/P B)	460	*	N/U	N/U
61	Clock ckt 6(T/P C)	461	*	N/U	N/U
62	Clock ckt 7(T/P D)	462	*	N/U	N/U
63	Pre-empt in 6	463	*	*	*

Communication Inputs Connector LMD9200 Pin Termination Assignments:

PIN #	LMD9200 FUNCTION	I/O REF NUMBER	MODE FUNCTIONS MODE 0	MODE 1	MODE 2
E-01	Vehicle Det. 17	465	*	*	*
E-02	Vehicle Det. 18	466	*	*	*
E-03	Vehicle Det. 19	467	*	*	*
E-04	Vehicle Det. 20	468	*	*	*
E-05	Vehicle Det. 21	469	*	*	*
E-06	Vehicle Det. 22	470	*	*	*
E-07	Vehicle Det. 23	471	*	*	*
E-08	Vehicle Det. 24	472	*	*	*
E-09	Monitor Status B	473	*	*	*
E-10	Monitor Status A	474	*	*	*
E-11	Monitor Status C	475	*	*	*
E-12	User Defined 1	476	*	*	*
E-14	User Defined 2	478	*	*	*
E-15	User Defined 3	479	*	*	*

Special Function Inputs LMD9200 Pin Termination Assignments:

PIN #	LMD9200 FUNCTION	I/O REF NUMBER	MODE FUNCTIONS MODE 0	MODE 1	MODE 2
N/A	Special Funct. 1	161	*	*	*
N/A	Special Funct. 2	162	*	*	*
N/A	Special Funct. 3	163	*	*	*
N/A	Special Funct. 4	164	*	*	*
N/A	Special Funct. 5	165	*	*	*
N/A	Special Funct. 6	166	*	*	*
N/A	Special Funct. 7	167	*	*	*
N/A	Special Funct. 8	168	*	*	*
N/A	Special Funct. 9	169	*	*	*
N/A	Special Funct. 10	170	*	*	*
N/A	Special Funct. 11	171	*	*	*
N/A	Special Funct. 12	172	*	*	*
N/A	Special Funct. 13	173	*	*	*
N/A	Special Funct. 14	174	*	*	*
N/A	Special Funct. 15	175	*	*	*
N/A	Special Funct. 16	176	*	*	*
N/A	Special Funct. 17	177	*	*	*
N/A	Special Funct. 18	178	*	*	*
N/A	Special Funct. 19	179	*	*	*
N/A	Special Funct. 20	180	*	*	*
N/A	Special Funct. 21	181	*	*	*
N/A	Special Funct. 22	182	*	*	*
N/A	Special Funct. 23	183	*	*	*
N/A	Special Funct. 24	184	*	*	*

Load Switch BIUs (Bus Interface Units) 1-4 LMD9200 Pin Termination Assignments:

PIN # /NAME	BIU # 1	BIU # 2	BIU # 3	BIU # 4
2a Output 1	1001 Chn01Red	1053 Chn09Red	1105 TimePlanAO	1157 Phs1PhsOn
2b Output 2	1002 Chn01Yel	1054 Chn09Yel	1106 TimePlanBO	1158 Phs2PhsOn
3a Output 3	1003 Chn01Grn	1055 Chn09Grn	1107 TimePlanCO	1159 Phs3PhsOn
3b Output 4	1004 Chn02Red	1056 Chn10Red	1108 TimePlanDO	1160 Phs4PhsOn
4a Output 5	1005 Chn02Yel	1057 Chn10Yel	1109 Offset1O	1161 Phs5PhsOn
4b Output 6	1006 Chn02Grn	1058 Chn10Grn	1110 Offset2O	1162 Phs6PhsOn
5a Output 7	1007 Chn03Red	1059 Chn11Red	1111 Offset3O	1163 Phs7PhsOn
5b Output 8	1008 Chn03Yel	1060 Chn11Yel	1112 AutoFlashO	1164 Phs8PhsOn
6a Output 9	1009 Chn03Grn	1061 Chn11Grn	1113 SysSpclF01	1165 Phs1PhsNxt
6b Output 10	1010 Chn04Red	1062 Chn12Red	1114 SysSpclF02	1166 Phs2PhsNxt
7a Output 11	1011 Chn04Yel	1063 Chn12Yel	1115 SysSpclF03	1167 Phs3PhsNxt
7b Output 12	1012 Chn04Grn	1064 Chn12Grn	1116 SysSpclF04	1168 Phs4PhsNxt
8a Output 13	1013 Chn05Red	1065 Chn13Red	1117 --	1169 Phs5PhsNxt
8b Output 14	1014 Chn05Yel	1066 Chn13Yel	1118 --	1170 Phs6PhsNxt
9a Output 15	1015 Chn05Grn	1067 Chn13Grn	1119 --	1171 Phs7PhsNxt
9b Input/Output 1	1017 Chn06Red	1069 Chn14Red	1121 StatBitA1	1173 Phs8PhsNxt
10a Input/Output 2	1018 Chn06Yel	1070 Chn14Yel	1122 StatBitB	1174 Phs1Check
10b Input/Output 3	1019 Chn06Grn	1071 Chn14Grn	1123 StatBitC1	1175 Phs2Check
11a Input/Output 4	1020 Chn07Red	1072 Chn15Red	1124 StatBitA2	1176 Phs3Check
11b Input/Output 5	1021 Chn07Yel	1073 Chn15Yel	1125 StatBitB2	1177 Phs4Check
12a Input/Output 6	1022 Chn07Grn	1074 Chn15Grn	1126 StatBitC2	1178 Phs5Check
12b Input/Output 7	1023 Chn08Red	1075 Chn16Red	1127 RedRestM1	1179 Phs6Check
13a Input/Output 8	1024 Chn08Yel	1076 Chn16Yel	1128 RedRestM2	1180 Phs7Check
13b Input/Output 9	1025 Chn08Grn	1077 Chn16Grn	1129 OmtRedClr1	1181 Phs8Check
14a Input/Output 10	1026 TBCAux1	1078 TBCAux3	1130 OmtRedClr2	1182 Addr0
14b Input/Output 11	1027 TBCAux2	1079 SystemOut	1131 PedRecyc1	1183 Addr1
15a Input/Output 12	1028 Preempt1O	1080 Preempt3O	1132 PedRecyc2	1184 Addr2
15b Input/Output 13	1029 Preempt2O	1081 Preempt4O	1133 AltSeqA	1185 Addr3
16a Input/Output 14	1030 Preempt1I	1082 Preempt5O	1134 AltSeqB	1186 Addr4
16b Input/Output 15	1031 Preempt2I	1083 Preempt6O	1135 AltSeqC	1187 --
17a Input/Output 16	1032 TestA	1084 Preempt3I	1136 AltSeqD	1188 --
17b Input/Output 17	1033 TestB	1085 Preempt4I	1137 Phs1PhsOmt	1189 --
18a Input/Output 18	1034 AutoFlashI	1086 Preempt5I	1138 Phs2PhsOmt	1190 --
18b Input/Output 19	1035 Dim	1087 Preempt6I	1139 Phs3PhsOmt	1191 --
19a Input/Output 20	1036 MCE	1088 CNA2I	1140 Phs4PhsOmt	1192 --
19b Input/Output 21	1037 IntvAdv	1089 --	1141 Phs5PhsOmt	1193 --
20a Input/Output 22	1038 MinRecall	1090 --	1142 Phs6PhsOmt	1194 --
20b Input/Output 23	1039 ExtStart	1091 --	1143 Phs7PhsOmt	1195 --
21a Input/Output 24	1040 TBCOnLine	1092 --	1144 Phs8PhsOmt	1196 --
21b Input 1	1041 StopTime1	1093 InhMaxTrm1	1145 Phs1Hold	1197 Phs1PedOmt
22a Input 2	1042 StopTime2	1094 InhMaxTrm2	1146 Phs2Hold	1198 Phs2PedOmt
22b Input 3	1043 MaxIISel1	1095 LocalFlash	1147 Phs3Hold	1199 Phs3PedOmt
23a Input 4	1044 MaxIISel2	1096 MMUFlash	1148 Phs4Hold	1200 Phs4PedOmt
23b Input 5	1045 FrcOff1	1097 UDA1	1149 Phs5Hold	1201 Phs5PedOmt
24a Input 6	1046 FrcOff2	1098 UDA2	1150 Phs6Hold	1202 Phs6PedOmt
24b Input 7	1047 CNA1I	1099 Free	1151 Phs7Hold	1203 Phs7PedOmt
25a Input 8	1048 WkRstMod	1100 TestC	1152 Phs8Hold	1204 Phs8PedOmt
25b Opto Input 1	1049 Ped1Det	1101 Ped5Det	1153 TimePlanAI	1205 Offset1I
26a Opto Input 2	1050 Ped2Det	1102 Ped6Det	1154 TimePlanBI	1206 Offset2I

Detector Rack BIUs (Bus Interface Units) 9-16 LMD9200 Pin Termination Assignments:

PIN # /NAME	BIU # 9	BIU # 10	BIU # 11	BIU # 12
2a Output 1	1417 DetRes00	1469 DetRes10	1521 DetRes20	1573DetRes30
2b Output 2	1418 DetRes01	1470 DetRes11	1522 DetRes21	1574 DetRes31
3a Output 3	1419 DetRes02	1471 DetRes12	1523 DetRes22	1575 DetRes32
3b Output 4	1420 DetRes03	1472 DetRes13	1524 DetRes23	1576 DetRes33
4a Output 5	1421 --	1473 --	1525 --	1577 --
4b Output 6	1422 --	1474 --	1526 --	1578 --
5a Output 7	1423 --	1475 --	1527 --	1579 --
5b Output 8	1424 --	1476 --	1528 --	1580 --
6a Output 9	1425 --	1477 --	1529 --	1581 --
6b Output 10	1426 --	1478 --	1530 --	1582 -
7a Output 11	1427 --	1479 --	1531 --	1583 --
7b Output 12	1428 --	1480 --	1532 --	1584 --
8a Output 13	1429 --	1481 --	1533 --	1585 --
8b Output 14	1430 --	1482 --	1534 --	1586 --
9a Output 15	1431 --	1483 --	1535 --	1587 --
9b Input/Output 1	1433 Veh01Det	1485 Veh17Det	1537 Veh33Det	1589 Veh49Det
10a Input/Output 2	1434 Veh02Det	1486 Veh18Det	1538 Veh34Det	1590 Veh50Det
10b Input/Output 3	1435 Veh03Det	1487 Veh19Det	1539 Veh35Det	1591 Veh51Det
11a Input/Output 4	1436 Veh04Det	1488 Veh20Det	1540 Veh36Det	1592 Veh52Det
11b Input/Output 5	1437 Veh05Det	1489 Veh21Det	1541 Veh37Det	1593 Veh53Det
12a Input/Output 6	1438 Veh06Det	1490 Veh22Det	1542 Veh38Det	1594 Veh54Det
12b Input/Output 7	1439 Veh07Det	1491 Veh23Det	1543 Veh39Det	1595 Veh55Det
13a Input/Output 8	1440 Veh08Det	1492 Veh24Det	1544 Veh40Det	1596 Veh56Det
13b Input/Output 9	1441 Veh09Det	1493 Veh25Det	1545 Veh41Det	1597 Veh57Det
14a Input/Output 10	1442 Veh10Det	1494 Veh26Det	1546 Veh42Det	1598 Veh58Det
14b Input/Output 11	1443 Veh11Det	1495 Veh27Det	1547 Veh43Det	1599 Veh59Det
15a Input/Output 12	1444 Veh12Det	1496 Veh28Det	1548 Veh44Det	1600 Veh60Det
15b Input/Output 13	1445 Veh13Det	1497 Veh29Det	1549 Veh45Det	1601 Veh61Det
16a Input/Output 14	1446 Veh14Det	1498 Veh30Det	1550 Veh46Det	1602 Veh62Det
16b Input/Output 15	1447 Veh15Det	1499 Veh31Det	1551 Veh47Det	1603 Veh63Det
17a Input/Output 16	1448 Veh16Det	1500 Veh32Det	1552 Veh48Det	1604 Veh64Det
17b Input/Output 17	1449 Veh01Flt	1501 Veh17Flt	1553 Veh33Flt	1605 Veh49Flt
18a Input/Output 18	1450 Veh02Flt	1502 Veh18Flt	1554 Veh34Flt	1606 Veh50Flt
18b Input/Output 19	1451 Veh03Flt	1503 Veh19Flt	1555 Veh35Flt	1607 Veh51Flt
19a Input/Output 20	1452 Veh04Flt	1504 Veh20Flt	1556 Veh36Flt	1608 Veh52Flt
19b Input/Output 21	1453 Veh05Flt	1505 Veh21Flt	1557 Veh37Flt	1609 Veh53Flt
20a Input/Output 22	1454 Veh06Flt	1506 Veh22Flt	1558 Veh38Flt	1610 Veh54Flt
20b Input/Output 23	1455 Veh07Flt	1507 Veh23Flt	1559 Veh39Flt	1611 Veh55Flt
21a Input/Output 24	1456 Veh08Flt	1508 Veh24Flt	1560 Veh40Flt	1612 Veh56Flt
21b Input 1	1457 Veh09Flt	1509 Veh25Flt	1561 Veh41Flt	1613 Veh57Flt
22a Input 2	1458 Veh10Flt	1510 Veh26Flt	1562 Veh42Flt	1614 Veh58Flt
22b Input 3	1459 Veh11Flt	1511 Veh27Flt	1563 Veh43Flt	1615 Veh59Flt
23a Input 4	1460 Veh12Flt	1512 Veh28Flt	1564 Veh44Flt	1616 Veh60Flt
23b Input 5	1461 Veh13Flt	1513 Veh29Flt	1565 Veh45Flt	1617 Veh61Flt
24a Input 6	1462 Veh14Flt	1514 Veh30Flt	1566 Veh46Flt	1618 Veh62Flt
24b Input 7	1463 Veh15Flt	1515 Veh31Flt	1567 Veh47Flt	1619 Veh63Flt
25a Input 8	1464 Veh16Flt	1516 Veh32Flt	1568 Veh48Flt	1620 Veh64Flt
25b Opto Input 1	1465 --	1517 --	1569 --	1621 --
26a Opto Input 2	1466 --	1518 --	1570 --	1622 --

NOTES:

LMD 9200 Series
Programming Charts

Revision 1.0.1 p/n MN-8976A

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AGENCY: _____

_____

PROGRAM DATE: _____ **INSTALLATION DATE:** _____

PROGRAMMED BY: _____

CONTROLLER SERIAL #: _____

SECURITY CODE: _____

IF COMM SYSTEM OR DIRECT DIAL:

ADDRESS: _____ **SECTION:** _____ **PHONE #:** _____

PEEK TRAFFIC SYSTEMS, INC.

LMD 9200 PROGRAMMING CHARTS

This chart set is intended for documentation of programming information provided by users for operation of the LMD9200 series traffic signal controller. An effort has been made to ensure the accuracy of the information contained in this chart set. However, the information is supplied without warranty of any kind. Further, there is no warranty of the applicability of the information to all cases. The user is cautioned to fully program and thoroughly test the controller for its intended application prior to placing it in operational service. PEEK Traffic Systems, Inc. reserves the right to add, delete, and/or modify the material in this chart set at any time.

RECALL MODES, BASE TIMINGS, PHASING & SEQUENCE, START-UP

MEMORY/RECALL/CNA (MM-2-2-1) Function values: ON or OFF

	ϕ1	ϕ2	ϕ3	ϕ4	ϕ5	ϕ6	ϕ7	ϕ8
MEMORY								
EXT RECALL								
MAX RECALL								
PED RECALL								
CNA I								
CNA II								
FLASH WALK								
SOFT RECALL								
ACT WALK REST								
COND. PED								
FWTPCL								

PHASE TIMING (MM-2-2-2)

	ϕ1	ϕ2	ϕ3	ϕ4	ϕ5	ϕ6	ϕ7	ϕ8
MIN GREEN								
PASSAGE								
YELLOW								
RED CLEAR								
MAX 1								
MAX 2								
WALK								
PED CLEAR								
S/A								
TBR								
TTR								
MIN GAP								
MAX VI								
MAX EXTEND								
AUTO MAX								
ADDED MAX RED								

Range: 0-9.9 or 127 except max times and auto max which are 0-255 secs

PHASES USED (MM-2-2-3-1)

PHASE	ϕ1	ϕ2	ϕ3	ϕ4	ϕ5	ϕ6	ϕ7	ϕ8
ON/OFF								

SEQUENCE (MM-2-2-3-2)

	1=Sequential, 2=Dual Ring, 3-7=Spec, 8 =Lead/Lag

LEAD/LAG MODES (MM-2-2-3-2-PGDN....only if Seq = Lead/lag)

PHASE	ϕ(1 & 2)	ϕ(3 & 4)	ϕ(5 & 6)	ϕ(7 & 8)
CODE				

Codes: 1 = No Reversal, 2 = Always Reverse, 3 = Rev. By CSO or Clock

LEAD/LAG BARRIERS (MM-2-2-3-2- PGDN- PGDN...only if lead/lag)

LEAD/LAG BARRIERS ARE:		ON/OFF

On = Barriers after each ring 1 and 2 phase pair in a vertical column

SPECIAL INCOMPATIBILITIES (MM-2-2-3-3)

PHASE	ϕ1	ϕ2	ϕ3	ϕ4	ϕ5	ϕ6	ϕ7	ϕ8
INCOMPAT PH 1-8								
INCOMPAT PH 1-8								

INITIALIZE/FLASH (MM-2-2-4) 1 = RED, 2 = YEL, 3=GRN

	INITIALIZE	ENTER FL	EXIT FLASH
RING 1 PHASE			
RING 2 PHASE			
INTERVAL		1	

NOTE: Enter flash interval is permanently set to 1 (RED)

POWER-UP RESTART TIMINGS (MM-2-2-4-PgDn)

MINIMUM FLASH		0 - 9.9 or 127 sec
1ST ALL RED AFTER FLASH		0 - 9.9 or 127 sec

NOTE: Blanks = 0, OFF, or controller default values

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OVERLAPS AND CONTROLLER OPTIONS

SET OVERLAPS (MM-2-2-5-1)

PHASE	ϕ1	ϕ2	ϕ3	ϕ4	ϕ5	ϕ6	ϕ7	ϕ8	
O/L A									0 = No Overlap
O/L B									1 = Standard
O/L C									2 = Fast FL O/L
O/L D									3 = Not Ped O/L

DELAYED OVERLAPS AND ADVANCED WARNING (MM-2-2-5-2)

	DEL	YEL	RED	CPH/OL	AW	ADD
O/L A				/		
O/L B				/		
O/L C				/		
O/L D				/		

DEL = Amount O/L yel delayed after parent ph (or advance warning time if used)
YEL = Yellow clearance for delayed O/L
RED = Red clearance for delayed O/L
CPH-OL = Conditional phase/O/L, used in advance warning if another phase or O/L would normally clear together with this O/L but has a longer delay (shorter advance assigns longer as conditional ph/O/L).
AW = 0 = Advance Warning not used (disabled), 1 = AW used (enabled)
ADD = Advance warning De-activation Delay; amount into green before warning signal shuts off (allows for Q's to exhaust after light turns green).

OVERLAP INHIBITS (MM-2-2-5-3)

PH-O/L	ϕ1	ϕ2	ϕ3	ϕ4	ϕ5	ϕ6	ϕ7	ϕ8	A	B	C	D
O/LA GRN												
O/LA YEL												
O/LA RED												
O/LB GRN												
O/LB YEL												
O/LB RED												
O/LC GRN												
O/LC YEL												
O/LC RED												
O/LD GRN												
O/LD YEL												
O/LD RED												

Apply code to inhibit indicated O/L colors:
0 = No Inhibit
1 = Inhibit during green
2 = Inhibit during yellow
3 = Inhib during red clr
4 = Inhib during grn & yel
5 = inhib during yel & red clr
6 = Inhibit during grn, yel, red clr
7 = Inhibit during wlk & ped clr

FAST FLASH RATE (MM-2-2-5-4)

	IN FPM: 0 = 6O, 1 = 120, 2 = 150, 3 =180

OVERLAP CARD (MM-2-2-5-5...Display only & only if O/L card installed)

O/L A PHASES	O/L B PHASES	O/L C PHASES	O/L D PHASES

PHASES AS OVERLAPS and ADVANCED WARNING (MM-2-2-5-6)

PH	1	2	3	4	5	6	7	8	DEL	CPH/OL	AW	AD
1										/		
2										/		
3										/		
4										/		
5										/		
6										/		
7										/		
8										/		

Row phase is phase as O/L, column phases are overlapping phases, where;
0 = No overlap (all 0's indicates row phase is a normal, non overlapping phase)
1 = Overlapping phase
.0 In delay column = Fast flash the overlap green

CPH = 1-8 = Phase 1-8
OL = 9-12 = OL A, B, C, D
ADD range = 0-99 sec

CONTROLLER OPTIONS

LAST CAR PASSAGE (MM-2-2-6-1)

ON REDUCED GAP OUT THE UNIT WILL	

1 = Recall phase, 2 = Last Car Passage, 3 = Terminate normally

SIMULTANEOUS GAP OUT INHIBIT (MM-2-2-6-1- PgDn)

PHASE	ϕ1	ϕ2	ϕ3	ϕ4	ϕ5	ϕ6	ϕ7	ϕ8
CODE								

0 = Passage can reset, 1 = passage cannot reset, 2 = input decides

DIMMING (MM-2-2-6-1-PgDn-PgDn)

PH-O/L	ϕ1	ϕ2	ϕ3	ϕ4	ϕ5	ϕ6	ϕ7	ϕ8	A	B	C	D
RED												
YEL												
GRN												
WLK									--	--	--	--
DW									--	--	--	--
PCL									--	--	--	--

0 = No Dim, 1 = Dim + half wave, 2 = Dim - half wave

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RED REVERT, PED OPTIONS, INCREASE YEL & RED (MM-2-2-6-2)

RED REVERT	PED ENHANCE MENT	FDW THRU YEL	AUTO PED CLEAR	% CKT 148 INC'S Y & R	TEST B
+ 2					

Red revert : Amount of red clear when phase "backs-up" on itself (+ 2 secs)
Ped Enhance: OFF = Normal walk time always used
ON = Normal walk time used if in CNA mode, max time used if not
FDW Thru Yel: OFF = Normal Flashing Don't Walk (goes solid when yellow starts)
ON = FDW continues thru yellow (time is added to PCL setting)
Auto Ped Clr: OFF = MCE does not protect ped clearances
ON = MCE does protect ped clearances
% Incr. Y & R: % amount Yellow & Red will be increased when clk ckt 148 is on
Test B input: Input used as: 0= DIM, 1= Call to free op, 2 = Call to free op after 3 minutes if input stays on

PED OVERLAPS (MM-2-2-6-2-PgDn)

PHASE	ϕ1	ϕ2	ϕ3	ϕ4	ϕ5	ϕ6	ϕ7	ϕ8	
PH 1 PED									
PH 2 PED									
PH 3 PED									
PH 4 PED									0 = NO PED
PH 5 PED									1 = PED O/L
PH 6 PED									
PH 7 PED									
PH 8 PED									

Allows peds to overlap phases. When a ped call exists, walk is initiated in 1st ped phase. If ped call exists on next overlapping ped phase, walk will be maintained into next phase, timing walk then ped clear if necessary in that phase.

0 = No overlap ped (note: if all 0's, ped is standard phase ped)
1 = Corresponding column phase is ped overlap parent phase

DUAL ENTRY (MM-2-2-6-3)

PHASE	ϕ1	ϕ2	ϕ3	ϕ4	ϕ5	ϕ6	ϕ7	ϕ8
DUAL ENTRY PHASE								

DUAL ENTRY MODE (MM-2-2-6-3-PgDn)

MODE	1 = OFF 3 = Called by CNA 5 = Called by Input
	2 = ON 4 = Called by system

CONDITIONAL SERVICE/RE-SERV (MM-2-2-6-3-PgDn-PgDn)

PHASE	ϕ1	ϕ3	ϕ5	ϕ7	
MODE					Mode range = 0-5 (see below)
C.S. MAX					C.S MAX = 0 - 99 secs

CS = Conditional Service, RS = Re-service (back to opposing thru after CS phase)

Mode:

0 = Both CS and RS OFF
1 = CS ON
2 = CS by clock or input
3 = CS If not system
4 = Both ON
5 = RS by clock or input

CS Max value determines if CS phase serviced, then acts as CS Max when green.
CS phase serviced if opposite thru phase gap's out when adjacent thru Max Time.
Remaining ≥ (Opposite Thru Clearance + CS MAX).

5 SECTION HEAD RESTRICTIONS (MM-2-2-6-4)

2 0MIT 5	4 0MIT 7	6 0MIT 1	8 0MIT 3	
				ON or OFF

5 SECTION HEAD YELLOW BLANKING (MM-2-2-6-4-PgDn)

PHASE	ϕ1	ϕ3	ϕ5	ϕ7	ON = Blanks yellow if clearing with adjacent through
ON or OFF					

NOTES

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SERVICE PLANS (MM-2-2-6-5-1-PgDn. etc.) Called by Clock or Cyc/Spl (plans override normal call modes, min grn, etc.)

SERVICE PLAN # 1								
PHASE	1	2	3	4	5	6	7	8
CALL MODE								
MIN GRN								
PASSAGE								
WLK								
PED CLR								

SERVICE PLAN # 4								
PHASE	1	2	3	4	5	6	7	8
CALL MODE								
MIN GRN								
PASSAGE								
WLK								
PED CLR								

SERVICE PLAN # 7								
PHASE	1	2	3	4	5	6	7	8
CALL MODE								
MIN GRN								
PASSAGE								
WLK								
PED CLR								

SERVICE PLAN # 2								
PHASE	1	2	3	4	5	6	7	8
CALL MODE								
MIN GRN								
PASSAGE								
WLK								
PED CLR								

SERVICE PLAN # 5								
PHASE	1	2	3	4	5	6	7	8
CALL MODE								
MIN GRN								
PASSAGE								
WLK								
PED CLR								

SERVICE PLAN # 8								
PHASE	1	2	3	4	5	6	7	8
CALL MODE								
MIN GRN								
PASSAGE								
WLK								
PED CLR								

SERVICE PLAN # 3								
PHASE	1	2	3	4	5	6	7	8
CALL MODE								
MIN GRN								
PASSAGE								
WLK								
PED CLR								

SERVICE PLAN # 6								
PHASE	1	2	3	4	5	6	7	8
CALL MODE								
MIN GRN								
PASSAGE								
WLK								
PED CLR								

SERVICE PLAN CALL MODES	
0 = OMIT	6 = PED RECALL
1 = ACTUATED	7 = PED OMIT
2 = CNA	
3 = RECALL EXT.	Note: Service plans called
4 = MAX RECALL	by clock ckt or Cyc/split.
5 = SOFT RECALL	Cyc/spl overrides clock

Each Service Plan used must be filled out entirely even if only one parameter is to be different from standard. All parameters indicated are invoked when the service plan is. **Also note** that if the call mode is "0," the phase will be omitted.

Value ranges: Call mode: 0-7 (see chart above) WLK: 0-9.9 or 127
MGR: 0-9.9 or 127 PCL: 0-9.9 or 127
PSG: 0-9.9 or 127

NOTES

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MAX PLANS (MM-2-2-6-5-2-PgDn, etc.) Called by Clock or Cyc/Spl (override normal max times when in effect)

MAX TIME MODE								
PHASE	1	2	3	4	5	6	7	8
MODE								
0 = use normal Nema times only, 1 = allow max plan selection by TOD/Coord								

1. Normal max is used when a plan is in effect with no detector failures.
2. Fail Max is used when a max plan is in effect and there is a failure on a detector and "Max Fail Recall" is applied to the phase (see det. monitoring)
3. Cyc/Spl overrides clock ckt when both are calling for a max time plan.

MAX TIME PLAN 1								
PHASE	1	2	3	4	5	6	7	8
NORMAL MAX								
FAIL MAX								

MAX TIME PLAN 2								
PHASE	1	2	3	4	5	6	7	8
NORMAL MAX								
FAIL MAX								

MAX TIME PLAN 3								
PHASE	1	2	3	4	5	6	7	8
NORMAL MAX								
FAIL MAX								

MAX TIME PLAN 4								
PHASE	1	2	3	4	5	6	7	8
NORMAL MAX								
FAIL MAX								

MAX TIME PLAN 5								
PHASE	1	2	3	4	5	6	7	8
NORMAL MAX								
FAIL MAX								

MAX TIME PLAN 6								
PHASE	1	2	3	4	5	6	7	8
NORMAL MAX								
FAIL MAX								

MAX TIME PLAN 7								
PHASE	1	2	3	4	5	6	7	8
NORMAL MAX								
FAIL MAX								

MAX TIME PLAN 8								
PHASE	1	2	3	4	5	6	7	8
NORMAL MAX								
FAIL MAX								

Value ranges: 0-255 seconds

NOTES

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DETECTOR ASSIGNMENTS

MEMORY/CALL/EXTEND ASSIGNMENTS (MM-2-2-6-6-1)

DETECTOR 1-8 Memory = ON/OFF, Call Phase & Ext/Sw = 1-8

DETECTOR	1	2	3	4	5	6	7	8
MEMORY								
CALL PHASE								
EXT/SWITCH PH	/	/	/	/	/	/	/	/

DETECTOR 9-16

DETECTOR	9	10	11	12	13	14	15	16
MEMORY								
CALL PHASE								
EXT/SWITCH PH	/	/	/	/	/	/	/	/

DETECTOR 17-24

DETECTOR	17	18	19	20	21	22	23	24
MEMORY								
CALL PHASE								
EXT/SWITCH PH	/	/	/	/	/	/	/	/

STRETCH/DELAY/MODE ASSIGNMENTS (MM-2-2-6-6-2)

DETECTOR 1-8 Delay, stretch, disconnect range: 0-9.9 or 127

DETECTOR	1	2	3	4	5	6	7	8
DELAY								
STRETCH/DISC.								
MODE								

Mode: 0 = norm delay & stretch. 1-8 = delay enable, 9 = 3rd row is disconnect val.

DETECTOR 9-16

DETECTOR	9	10	11	12	13	14	15	16
DELAY								
STRETCH/DISC.								
MODE								

DETECTOR 17-24

DETECTOR	17	18	19	20	21	22	23	24
DELAY								
STRETCH/DISC.								
MODE								

DETECTOR FAIL MONITOR (MM-2-2-6-6-3, PGDN etc.)

Phase assigned is placed in fail max recall if det fails. Min/max are counts allowed over sample period.

DETECTOR FAIL SAMPLE PERIOD

	0-255 MINUTES

DETECTOR FAIL MONITOR MODE, DET'S 1-8

DETECTOR	1	2	3	4	5	6	7	8
MODE (ON/OFF)								

DETECTOR FAIL MONITOR MODE, DET'S 9-16

DETECTOR	9	10	11	12	13	14	15	16
MODE (ON/OFF)								

DETECTOR FAIL MONITOR MODE, DET'S 17-24

DETECTOR	17	18	19	20	21	22	23	24
MODE (ON/OFF)								

DETECTOR FAIL MONITOR ASSIGNMENT DET'S 1-8

DETECTOR	1	2	3	4	5	6	7	8
PHASE								
MIN (0-999)								
MAX (0-999)								

DETECTOR FAIL MONITOR ASSIGNMENT DET'S 9-16

DETECTOR	9	10	11	12	13	14	15	16
PHASE								
MIN ((0-999)								
MAX (0-999)								

DETECTOR FAIL MONITOR ASSIGNMENT DET'S 17-24

DETECTOR	17	18	19	20	21	22	23	24
PHASE								
MIN (0-999)								
MAX (0-999)								

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DETECTOR SIMULATION NOTE: For Testing Only Not a Field Function.

DETECTOR SIMULATION MODE (MM-2-2-6-6-4)

MODE	

0 = OFF, 1= Input and system level, 2= System level only

DETECTOR VOLUMES (MM-2-2-6-6-4-PGDN, etc.)

DET	1	2	3	4	5	6
SAT FLOW						
PRCNT SAT						
*TOTAL VOL						

DET	7	8	9	10	11	12
SAT FLOW						
PRCNT SAT						
*TOTAL VOL						

DET	13	14	15	16	17	18
SAT FLOW						
PRCNT SAT						
*TOTAL VOL						

DET	19	29	21	22	23	24
SAT FLOW						
PRCNT SAT						
*TOTAL VOL						

SAT FLOW = Vehicles per hour, max volume when flow unimpeded.

PRCNT SAT = % of above vehicle per hour rate used to compute volume.

*TOTAL VOL = NOT AN ENTRY, computed by LMD based on above % of SAT.

DET PULSE WIDTH & GATE PH'S (MM-2-2-6-6-4-PGDN, etc.)

DET	1	2	3	4	5	6
PULSE MS						
GATE PHS						

DET	7	8	9	10	11	12
PULSE MS						
GATE PHS						

DET	13	14	15	16	17	18
PULSE MS						
GATE PHS						

DET	19	20	21	22	23	24
PULSE MS						
GATE PHS						

PULSE MS = Duration of each call pulse in Milliseconds (1000 = 1 sec).

GATE PHS RANGE: 1-8 = Phase 1-8, 9-12 = Overlap A-D

Note: Gate phases cause simulation to act like a real stop bar detector. Rather than just issue calls continuously at a fixed rate, the calls are accumulated when the gate phase (or overlap) is red, then discharges them after the phase is green.

QUEUE DET & QUEUE COUNT (MM-2-2-6-6-4-PGDN, etc.)

DET	1	2	3	4	5	6	7	8
QUE DET								
QUE CNT								

DET	9	10	11	12	13	14	15	16
QUE DET								
QUE CNT								

DET	17	18	19	20	21	22	23	24
QUE DET								
QUE CNT								

QUE DET = Designated DET that is "upstream" from primary DET (column head)
QUE CNT = Number of counts (during red) on QUE DET before it goes steady on (as if vehicles backed up to it and stopped). Can be used for Adaptive Split.

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COORDINATION

COORD MODES (MM-2-3-1) Determines selection mode

FL		ON/OFF 9=TC 10=INT 11=COM 12=AU
SYS		ON/OFF 9=TC 10=INT 11=COM 12=AU
CYC		1-8=MAN 9=TC 10=INT 11=COM 12=AU
SPL		1-4=MAN 9=TC 10=INT 11=COM 12=AU
OFF		0-5=MAN 9=TC 10=INT 11=COM 12=AU

OFFSET SEEKING MODE (MM-2-3-2)

SEEKING MODE	0 =Manual resync (hit clr in coord run screen)
	1 =Dwell, 2 = shortway, 3 = interrupter

COORD OPTIONS

Note: Floating force offs cause force off values to act like max times, not points in cycle. SCM causes cycle timer to stop & wait if phase can't be forced off--like when a ped is timing. Walk adjust causes the unit to "look ahead," to see if the ped will terminate before the force off point. If not (like when offset seeking), it will shorten the walk as needed, to as low as 10 sec.

OPERATIONAL (MM-2-3-3-1)

FLOAT F.O'S	LOSS SYNC TO FREE	SYS TO MX2	SYS TO CNA	CSO / FREE	SCM MODE	WALK ADJ

All options ON or OFF except CSO/Free which is 0 or 111 - 956 (don't cares)
Floating force offs = 3 = Special code, fixed F.O. but no CNA ph force offs

CSO TO LEAD/LAG PATTERNS (MM-2-3-3-2)

SEQ	CSO	1 & 2	3 & 4	5 & 6	7 & 8	
1						1 = ODD LEADS
2						
3						2 = ODD LAGS
4						
5						
6						9, 5, 6 = Don't care states for C, S, O
7						
8						
9						
10						

ADAPTIVE SPLIT (MM-2-3-3-3-PgDn, etc.)

CYCLES		Number of cycles used per adaptive split sample
MODE		How Ad. split selected: 0=Queues, 1=Force offs
THRSH		Min # of queues or force offs to select new split

ADAPTIVE SPLIT TO PHASE ASSIGNMENTS (MM-2-3-3-3-PgDn, etc.)

SPL /PH	ϕ1	ϕ2	ϕ3	ϕ4	ϕ5	ϕ6	ϕ7	ϕ8	
1									0 =Not considered
2									
3									1 =Selected phases
4									

QUEUE DETECTOR TO PHASE ASSIGNMENTS (MM-2-3-3-3-PgDn, etc.)

PHASE	1	1	2	2	3	3	4	4
Q. DETECTOR								
Q. DELAY								

PHASE	5	5	6	6	7	7	8	8
Q. DETECTOR								
Q. DELAY								

Q DET Ranges: Q detector =1-24, Q delay = 0-9.9 or 127,

ADAPTIVE SPLIT INHIBITS (MM-2-3-3-3-PgDn, etc.)

CYC 1	O1	O2	O3	Q4	O5
SPL 2					
SPL 3					
SPL 4					

CYC 5	O1	O2	O3	O4	O5
SPL 2					
SPL 3					
SPL 4					

CYC 2	O1	O2	O3	Q4	O5
SPL 2					
SPL 3					
SPL 4					

CYC 6	O1	O2	O3	O4	O5
SPL 2					
SPL 3					
SPL 4					

CYC 3	O1	O2	O3	Q4	O5
SPL 2					
SPL 3					
SPL 4					

CYC 7	O1	O2	O3	O4	O5
SPL 2					
SPL 3					
SPL 4					

CYC 4	O1	O2	O3	Q4	O5
SPL 2					
SPL 3					
SPL 4					

CYC 8	O1	O2	O3	O4	O5
SPL 2					
SPL 3					
SPL 4					

0 = No inhibit, 1 = inhibit (do not allow split to be selected during that cyc & offset)

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CSO TO TIME CLK CKT MAPPING (MM-2-3-3-4-PgDn, etc.)

CS0 / S	Ckt	Ckt	Ckt	Ckt	Ckt	Ckt	Ckt	Ckt
/								
/								
/								
/								
/								
/								
/								
/								
/								
/								

CSO/S = Combination of Cycle, Split, Offset, and System status to call clock ckts
Ranges: CSO: 111 - 956 (956 =Don't cares), S: 0 = Don't care, 1= sys, 2=not sys
CKTS = Clock ckts 9-12, 14-150

COORD PH/SERVICE/MAX PLAN ASSIGNMENTS (MM-2-3-4)

CYC 1	S1	S2	S3	S4
COORD PH's				
SERVICE PL				
MAX PLAN				

CYC 2	S1	S2	S3	S4

CYC 3	S1	S2	S3	S4
COORD PH's				
SERVICE PL				
MAX PLAN				

CYC 4	S1	S2	S3	S4

CYC 5	S1	S2	S3	S4
COORD PH's				
SERVICE PL				
MAX PLAN				

CYC 6	S1	S2	S3	S4

CYC 7	S1	S2	S3	S4
COORD PH's				
SERVICE PL				
MAX PLAN				

CYC 8	S1	S2	S3	S4

Coord phases are always 2 digits; ring1 & ring2, e.g. 10 =ph 1 only, 26 =ph's 2 & 6
Ranges; Coord phases = 0-88 Service plan = 0-8 Max plan = 0-8

CYCLE LENGTH/MAX DWELL (MM-2-3-5)

CYCLE	1	2	3	4	5	6	7	8
LENGTH								
MAX DWL								

Range: 0-255 seconds

OFFSETS (MM-2-3-5-PgDn)

OFFSET	1	2	3	4	5
CYC 1					
CYC 2					
CYC 3					
CYC 4					
CYC 5					
CYC 6					
CYC 7					
CYC 8					

Range: 0-255 seconds

NOTES

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FORCE OFFS AND PERMISSIVES, MANUAL ENTRY

PED PERM, PERM MODE (MM-2-3-6-1-1)

PED PERM	1-255 SECS or	PERM MODE	0 = STANDARD
	0 = AUTO CALC		1 = STRICT

Standard permissives deactivate after leaving coord phase (recommended mode)
Strict perms operate strictly by on/off programming, regardless of active phase

FORCE OFF TO PHASE ASSOCIATIONS (MM-2-3-6-1-2)

FORCE OFF	1	2	3	4	5	6	7	8
PHASE(S)								

MANUAL FORCE OFF TIMES (MM-2-3-6-1-2-PgDn, etc.)

	F.O.	1	2	3	4	5	6	7	8
C1	SPL 1								
	SPL 2								
	SPL 3								
	SPL 4								

	F.O.	1	2	3	4	5	6	7	8
C2	SPL 1								
	SPL 2								
	SPL 3								
	SPL 4								

	F.O.	1	2	3	4	5	6	7	8
C3	SPL 1								
	SPL 2								
	SPL 3								
	SPL 4								

	F.O.	1	2	3	4	5	6	7	8
C4	SPL 1								
	SPL 2								
	SPL 3								
	SPL 4								

Range: 0-255 seconds

MANUAL FORCE OFF TIMES CONTINUED....

	F.O.	1	2	3	4	5	6	7	8
C5	SPL 1								
	SPL 2								
	SPL 3								
	SPL 4								

	F.O.	1	2	3	4	5	6	7	8
C6	SPL 1								
	SPL 2								
	SPL 3								
	SPL 4								

	F.O.	1	2	3	4	5	6	7	8
C7	SPL 1								
	SPL 2								
	SPL 3								
	SPL 4								

	F.O.	1	2	3	4	5	6	7	8
C8	SPL 1								
	SPL 2								
	SPL 3								
	SPL 4								

MANUAL PERMISSIVE TO PH ASSOCIATIONS (MM-2-3-6-1-3)

PERMISSIVE	1	2	3	4
PHASE(S)				

PERMISSIVE	5	6	7	8
PHASE(S)				

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MANUAL PERMISSIVE TIMES (MM-2-3-6-1-3-PgDn, etc.)

CYC1 PERM	1	2	3	4	5	6	7	8
S1 START								
END								
S2 START								
END								
S3 START								
END								
S4 START								
END								

CYC2 PERM	1	2	3	4	5	6	7	8
S1 START								
END								
S2 START								
END								
S3 START								
END								
S4 START								
END								

CYC3 PERM	1	2	3	4	5	6	7	8
S1 START								
END								
S2 START								
END								
S3 START								
END								
S4 START								
END								

CYC4 PERM	1	2	3	4	5	6	7	8
S1 START								
END								
S2 START								
END								
S3 START								
END								
S4 START								
END								

Range: 0-255 seconds

MANUAL PERMISSIVE TIMES CONTINUED...

CYC5 PERM	1	2	3	4	5	6	7	8
S1 START								
END								
S2 START								
END								
S3 START								
END								
S4 START								
END								

CYC6 PERM	1	2	3	4	5	6	7	8
S1 START								
END								
S2 START								
END								
S3 START								
END								
S4 START								
END								

CYC7 PERM	1	2	3	4	5	6	7	8
S1 START								
END								
S2 START								
END								
S3 START								
END								
S4 START								
END								

CYC8 PERM	1	2	3	4	5	6	7	8
S1 START								
END								
S2 START								
END								
S3 START								
END								
S4 START								
END								

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AUTO CALC SPLIT PERCENTAGES (MM-2-3-6-2-1-1-PgDn, etc.)

PHASE	1	2	3	4	5	6	7	8
C1 SPLIT 1								
SPLIT 2								
SPLIT 3								
SPLIT 4								

PHASE	1	2	3	4	5	6	7	8
C2 SPLIT 1								
SPLIT 2								
SPLIT 3								
SPLIT 4								

PHASE	1	2	3	4	5	6	7	8
C3 SPLIT 1								
SPLIT 2								
SPLIT 3								
SPLIT 4								

PHASE	1	2	3	4	5	6	7	8
C4 SPLIT 1								
SPLIT 2								
SPLIT 3								
SPLIT 4								

PHASE	1	2	3	4	5	6	7	8
C5 SPLIT 1								
SPLIT 2								
SPLIT 3								
SPLIT 4								

PHASE	1	2	3	4	5	6	7	8
C6 SPLIT 1								
SPLIT 2								
SPLIT 3								
SPLIT 4								

Range: 0-99% of cycle length

AUTO-CALC PERMISSIVE TIMES CONTINUED...

PHASE	1	2	3	4	5	6	7	8
C7 SPLIT 1								
SPLIT 2								
SPLIT 3								
SPLIT 4								

PHASE	1	2	3	4	5	6	7	8
C8 SPLIT 1								
SPLIT 2								
SPLIT 3								
SPLIT 4								

AUTO CALC PERMISSIVE TYPES (MM-2-3-6-2-2)

TYPE		0 = Yield, 1 = Single, 2 = Multiple
MODE		0/1 = Start/end the coord phase at the cycle 0 point
EGB%		0-99% =Coord phase extendible green band percent

AUTO CALC NORMAL vs. CNA OPTION (MM-2-3-6-2-3)

MODE		0 = normal, no CNA 1 = CNA used on coord phases

NOTES

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TIME CLOCK

DAYLIGHT SAVINGS, RESET TIME, COORD OUT (MM-2-4-2)

DLS (ON/OFF)	CLOCK RESET TIME	COORD OUT
	: :	

DLS: ON = Clock will spring forward and fall back automatically for DLS
OFF = Clock will not adjust for daylight savings

Clock Reset Time = Time of day the clock will be set to on "time clock sync" input toggle (trailing edge)

Coord: 0 = Coord outputs follow only TOD coord clock programming regardless of actual select mode

1 = Coord outputs follow active coord commands unit is responding to (TOD, INT, COMM)

SYNC REFERENCE MODE (MM-2-4-3)

MODE

Determines how clock derives coord cycle sync pulses from time base (2 = most common mode used):

1 = End of previous cycle (1st sync at midnight, then each new selected cycle references to end of current cycle--this mode is event history sensitive)

2 = Independent daily reference (each cycle has own, independent reference back to daily cycle zero time--this mode is not event history sensitive)

3 = Absolute reference (one time reference, then runs continuous w/no daily resync, usually used to sync to free running electro-mechanical dials)

4 = Event reference (cycle timer resyncs to zero each time a new cycle called for by clock event--this mode is event history sensitive)

INDEPENDENT CYCLE ZERO TIMES (MM-2-4-3-PgDn)

C1 : :	C2 : :	C3 : :
C4 : :	C5 : :	C6 : :
C7 : :	C8 : :	/ / / / / / / / / / / /

Range: 6 digit time of day. 00:00:00 to 23:59:59

EXCEPTION DAYS (MM-2-4-4) (DP = Day Program)

DESCRIPTION	EX DAY	DOW	WOM	or DOM	MOY	DP
	1					
	2					
	3					
	4					
	5					
	6					
	7					
	8					
	9					
	10					
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34					
	35					

Use DOM, MOY for date specific events (Christmas), Use DOW WOM for events that fall on a specific day of a certain week (e.g. "Monday Holidays").

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TIME CLOCK CKT MODES (MM-2-4-5-PgDn, etc.)

MODE = ON/OFF or AUTO (BLANK = AUTO)

CKT	8	9	10	11	12	13	14	15
FUNCT	FL	AX1	AX2	AX3	AX4	SYS	MX2	IM1
MODE	N/A					N/A		

CKT	16	17	18	19	20	21	22	23
FUNCT	IM2	CN1	CN2	MIN	VC1	VC2	VC3	VC4
MODE								

CKT	24	25	26	27	28	29	30	31
FUNCT	VC5	VC6	VC7	VC8	PC1	PC2	PC3	PC4
MODE								

CKT	32	33	34	35	36	37	38	39
FUNCT	PC5	PC6	PC7	PC8	VO1	VO2	VO3	VO4
MODE								

CKT	40	41	42	43	44	45	46	47
FUNCT	VO5	VO6	VO7	VO8	PO1	PO2	PO3	PO4
MODE								

CKT	48	49	50	51	52	53	54	55
FUNCT	PO5	PO6	PO7	PO8	CSV	SGO	INT	SYN
MODE								

CKT	56	57	58	59	60	61	62	63
FUNCT	WRM	DLE	RR1	RR2	OR1	OR2	PR1	PR2
MODE								

CKT	64	65	66	67	68	69	70	71
FUNCT	DL1	DPI	PE1	PE2	PE3	PE4	PE5	PE6
MODE								

CKT	72	73	74	75	76	77	78	79
FUNCT	MP1	MP2	MP3	MP4	MP5	MP6	MP7	MP8
MODE								

Range: ON/OFF/AUTO. On = manually on, Off = manually off, Auto =time of day

CKT	80	81	82	83	84	85	86	87
FUNCT	SP1	SP2	SP3	SP4	SP5	SP6	SP7	SP8
MODE								

CKT	88	89	90	91	92	93	94	95
FUNCT	LG1	LG3	LG5	LG7	VD1	VD2	VD3	VD4
MODE								

CKT	96	97	98	99	100	101	102	103
FUNCT	VD5	VD6	VD7	VD8	EXP	I17	I18	I19
MODE								

CKT	104	105	106	107	108	109	110	111
FUNCT	I20	I21	I22	I23	I24	ASC	OLA	OLB
MODE								

CKT	112	113	114	115	116	117	118	119
FUNCT	OLC	OLD	AT1	AT2	BT1	BT2	CT1	CT2
MODE								

CKT	120	121	122	123	124	125	126	127
FUNCT	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8
MODE								

CKT	128	129	130	131	132	133	134	135
FUNCT	ID9	I10	I11	I12	I13	I14	I15	I16
MODE								

CKT	136	137	138	139	140	141	142	143
FUNCT	EAV	VT1	VT2	EVL	EAM	EML	ICP	IDD
MODE								

CKT	144	145	146	147	148	149	150
FUNCT	CTF	DEP	I5H	CTC	IYR	DIM	W10
MODE							

Range: ON/OFF/AUTO. On = manually on, Off = manually off, Auto =time of day

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TIME CLOCK WEEK PROGRAM (MM-2-4-6-PgDn, etc.)

WEEK PROGRAM	S	M	T	W	T	F	S
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							

Assign day programs 1-15 to each day of week

TIME CLOCK YEAR PROGRAM (MM-2-4-7)

FROM DATE	TO DATE	WEEK PROG 1-10

NOTES

TIME CLOCK DAY PROGRAMS (MM-2-4-8)

DAY PROG	EVENT TIME	CSO	or CKT (ON/OFF)
	: :		
	: :		
	: :		
	: :		
	: :		
	: :		
	: :		
	: :		
	: :		
	: :		
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	: :		

NOTE: Ckt 13 calls for system (coord) operation

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LIST OF TIME CLOCK CKTS AND THEIR FUNCTION

CKT#	ABBREV	FUNCTION
8	FL	Remote (UCF) flash--see Initialize/Flash, Coord
9-12	AX1-4	Auxiliary, general purpose clock outputs
13	SYS	Call for system (coordinated) operation
14	MX2	Call Max 2 timing (both rings)
15,16	IM1,2	Inhibit Max ring 1 & 2
17,18	CN1,2	Call to non-act 1 & 2
19	MIN	Minimum timing recall to all phases
20-27	VC1-8	Vehicle call phases 1-8
28-35	PC1-8	Ped call phases 1-8
36-43	VO1-8	Vehicle omit phases 1-8
44-51	PO1-8	Ped omit phases 1-8
52	CSV	Call for conditional service (CS in clock mode)
53	SGO	Call for SGOInh (psg timer can't restart after gap)
54	INT	Interconnect inhibit (enable clock for coord select)
55	SYN	Sync inhibit (makes offset outputs steady state)
56	WRM	Walk Rest Modifier (CNA rest in wlk after hold released if no calls)
57	DLE	Enable Dual Entry if DLE in clock mode (one ph calls another--see dual entry)
58, 59	RR1,2	Red rest mode ring 1 and 2 (rests in red)
60, 61	OR1,2	Omit red clear ring 1 and 2. Red clear skipped
62,63	PR1,2	Ped recycle rings 1 and 2 (see manual for def.)
64	DLI	Detector low & no counts monitoring inhibit.
65	DPI	Detector presence ("constant call") mon inhibit.
66-71*	PE1-6	Pre-empt 1-6 call.
72-79	MP1-8	Max Plan 1-8. Calls indicated max plan
80-87	SP1-8	Service Plan 1-8. Calls indicated Service plan.
88-91	LG1,3,5,7	Lead/Lag phase reversals (1-2, 3-4, 5-6, 7-8)
92-99	VD1-8	Inhibit volume density (gap reduction) per phase
100	EXP	Exclusive ped. Ph's 2, 4, 6, 8 peds all come on after 2 & 6 using ph 1 timing.
101-108	I17-24	Inhibit detectors 17-24
109	ASC	Adaptive split control, When on, split derived from veh Q's or veh demand
110-113	OLA-D	Inhibit overlap A-D. When inhibited, O/L will clear using own yellow, remain red then remains off
114,115	AT1,2	Enable call in of "A" messages to phone # 1, 2
116,117	BT1,2	Enable call in of "B" messages to phone # 1, 2
118,119	CT1,2	Enable call in of "C" messages to phone # 1, 2
120-135	ID1-I16	Inhibit detectors 1-16
136	EAV	Enable alternate volume sampling period
137,138	VT1,VT2	Enable call in of volume logs to phone # 1, 2
139	EVL	Enable volume logging
140	EAM	Enable alternate MOE sampling period
141	EML	Enable MOE logging
142	ICP	Inhibit conditional ped. Disallows late or 2nd ped
143	IDD	Inhibit detector delay all detectors
144	CTF	Call to free--overrides all other modes of coord
145	DEP	Dual enhanced ped. First wlk (say ph 2) waits for 2nd wlk (say ph 6), then go to PCL together
146	I5H	Inhibit 5 section head logic
147	CTC	Call to clock--overrides all other modes of coord
148	IYR	Increase yellow in red by % amount
149	DIM	Enables G-Y-R-W-DW dimming per programming
150	W10	Call to week program 10 (overrides normal WP)

***Note that** when priority pre-empt mode is enabled, clock ckts 66-68 select PRB-D percents. CKT 69 inhibits priority return operation.

NOTES

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PRE-EMPTION

PRE-EMPT 1-3 SEQUENCE STEPS (MM-2-5-(1-3))

SEQ1	PHS-SPECL	TIME	HOI	OUTPUTS
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				

SEQ3	PHS-SPECL	TIME	HOI	OUTPUTS
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				

SEQ2	PHS-SPECL	TIME	HOI	OUTPUTS
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				

SEQUENCE CODES:

1-8 = Phases 1-8 allowed
.1-.9 = Special intervals
89 = Hold on input w/gap
90 = Go to All Red
91 = CVM OFF (flash)
92 = CVM ON
93 = Enable Peds
94 = Inhibit peds
95 = Priority return phases
96 = Enable coordination
97 = Strict permissives
98 = Exit, no calls
99 = Exit, ped calls all ph's

T IME = 0-9.9 or 127 secs
Acts as min time if HOI = ON
Acts as step time if HOI = OFF

Note: If Time =0 for first step, any outputs come on with input **If Time =.0** for first step, barrier phases in different rings can clear independently. Otherwise they wait until they both can clear. **If Time =0 for 95** priority return instruction, it is actually .2 secs

HOI = "Hold on Input" (On or Off)

Outputs = Pre-empt outputs activated during that step:

1-6 = PE 1-6 out
7 = Flash suffix (e.g. 17 = flash PE output 1)

Note: Low priority steps for a given pre-empt input start at step 10. That is, when activated by Low Priority (pulsing input), the sequence is entered at step 10, then goes to 11, etc.

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PRE-EMPT 4-6 SEQUENCE STEPS (MM-2-5-(4-6))

SEQ4	PHS-SPECL	TIME	HOI	OUTPUTS
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				

SEQ5	PHS-SPECL	TIME	HOI	OUTPUTS
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				

SEQ6	PHS-SPECL	TIME	HOI	OUTPUTS
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				

SEQUENCE CODES:

1-8 = Phases 1-8 allowed
.1-.9 = Special intervals
89 = Hold on input w/gap
90 = Go to All Red
91 = CVM OFF (flash)
92 = CVM ON
93 = Enable Peds
94 = Inhibit peds
95 = Priority return phases
96 = Enable coordination
97 = Strict permissives
98 = Exit, no calls
99 = Exit, ped calls all ph's

T IME = 0-9.9 or 127 secs
Acts as min time if HOI = ON
Acts as step time if HOI = OFF

Note: If Time = 0 for first step, any outputs come on with input **If Time =.0** for first step, barrier phases in different rings can clear independently. Otherwise they wait until both can clear. **If Time = 0 for 95** priority return instruction, it actually times .2 secs

HOI = "Hold on Input" (On or Off)

Outputs = Pre-empt outputs activated during that step:

1-6 = PE 1-6 out
7 = Flash suffix (e.g. 17 = flash PE output 1)

Note: Low priority steps for a given pre-empt input start at step 10. That is, when activated by Low Priority (pulsing input), the sequence is entered at step 10, then goes to 11, etc.

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SPECIAL INTERVALS (MM-2-5-7) (BLANK = DEFAULT = CODE 5 = RED)

SPEC. INTERVAL	PH1	PH1	PH2	PH3	PH4	PH5	PH6	PH7	PH8	OL A	OL B	OL C	OL D
.1													
.2													
.3													
.4													
.5													
.6													
.7													
.8													
.9													

Phase and Overlap color codes
0 = Dark
1 = Green/dw
2 = Green/walk
3 = Flashing Don't Walk
4 = Yellow
5 = Red
6 = Flash Yellow Wig
7 = Flash Yellow Wag
8 = Flash Red Wig
9 = Flash Red Wag
. = Fast Flash green

Notes: 1. "Wig" and "Wag" are 180 degrees out of phase w/each other
2. Must enter special intervals from all red, i.e. "90" code must precede first special interval. The last interval must be all 5's.

HI PRIORITY PRE-EMPT SET-UP

PE MEMORY/DELAY/RE-SERVICE (MM-2-5-8-1)

PE INPUT	1	2	3	4	5	6
MEMORY (ON/OFF)						
DELAY BEFORE PE						
MIN RESEVICE						

Delay Range = 0-255 Seconds, Reservice = 0 - 99 Minutes

PE OVERLAP INHIBITS (MM-2-5-8-2)

PE INPUT	1	2	3	4	5	6

Use 4 digit code for each input in order of ABCD

0 = Allow normal overlap
1 = Inhibit overlap on entry into and during pre-empt

Example: 0100 = Inhibit OL/B

PRE-EMPT ENTRY TIMES (MM-2-5-8-3)

PE INPUT	MGR	WLK	PCL	OLY	OLR	FDW/Y
1						
2						
3						
4						
5						
6						

Range: 0 - 9.9 or 127 for MGR, WLK, PCL, OLY, OLR. FDW/Y = ON OFF

Note: "0" for MGR, WLK, PCL = Use normal phase time values. Thus, ".1" is the shortest programmable PE entry time for these values.

OLY, OLR = Overlap yellow & red time when OL must time its own clearance.
FDW/Y= ON = Allow Don't Walk to flash through yellow on entry into PE.

PRE-EMPT PRIORITIES (MM-2-5-8-4)

PE INPUT	1	2	3	4	5	6
PRIORITY						
OVERRIDE FLASH						

Priority = 1-6 (1 = highest, 6 = lowest). When equal, 1st come 1st serve.
Override Flash = ON/OFF. ON = Exit remote (UCF) flash for pre-empt.

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HOLD ONLY PRE-EMPT (MM-2-5-8-5)

PE INPUT	1	2	3	4	5	6
ON/OFF						
PHASES						
TIME						

When ON hold only operation in effect, no sequence steps required. Only holds phase if green when PE input active. Phases = one phase or a compatible phase pair. Hold time range = 0 - 9.9 or 127 secs.

PE DELAY OPTION (MM-2-5-8-6)

PE INPUT	1	2	3	4	5	6
PED OMIT LAST X						
VEH OMIT LAST X						

Range = 0 - 9.9 or 127 secs. Used when there is delay before pre-empt. Omits peds or phases during last x seconds of the delay period. Prevents late service to non pre-empt peds or phases just before delay times out.

PRIORITY RETURN ENABLE (MM-2-5-8-7)

MODE		ON/OFF: ON = Priority return Enabled OFF = Priority return Disabled
SKIP OPTION		ON/OFF: ON=Skip PE phase(s) 1st cycle after PE if next after return ph. OFF=Don't skip

PRIORITY RETURN PHASE MIN PERCENTS (MM-2-5-8-7-PgDn)

PHASE	1	2	3	4	5	6	7	8
PRA %								
PRB %								
PRC %								
PRD %								

Range: 0 - 100%. If "95" exit code used in sequence, will return back to preempted phase (when PE started) if phase has demand & was served less than above percent of its allocated time (max or coord split if auto-calc percents loaded)

Note: When priority mode ON (above), clock ckts 66-68 select PRB-D percent's. CKT 69 inhibits priority return operation.

PED PRIORITY RETURN MIN % (MM-2-5-8-7-PgDn 3 Times)

PHASE	1	2	3	4	5	6	7	8
PCL %								

Range: 0 - 100%. If "95" exit code used in sequence, will return back to ped of pre-empted phase (when PE started) if PED CLEAR was served less than above percent of its normal ped clear time.

LOW PRIORITY PRE-EMPT SET-UP

(MM-2-5-9-PgDn, etc.)

	MEM	MGR	WLK	PCL	OLY	OLR	DEL	OMT	RESV
LP1									
LP2									
LP3									
LP4									
LP5									
LP6									

MEM = ON/OFF,
Ranges: MGR, WLK, PCL, OLY, OLR, OMT (Last X) = 0 - 9.9 or 127 secs
DEL = 0 - 255 secs, Re-service = 0 - 99 min.

Notes:

1. LPE starts at sequence step 10 (see sequence steps note)
2. OMT (Last X) & Re-service have same function as HI PE

NOTES

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COMM SET-UP

SYSTEM PORT SET-UP (MM-2-6-1)

SYSTEM PORT		SYSTEM #	
SYSTEM TYPE		UNIT ADDRESS	

System Port: 0 = Fsk Modem, 1 = RS-232A, 2= RS-232B
System Type: 0 =LM100 (1200 baud), 1 - 4 = 1200, 2400, 4800, 9600 for MIST or MATS
System #: 0 - 99 = Master Zone ID number (automatic w/MDM100))
Unit Address: 0 - 64 = Unit address number

NON-SYSTEM PORT SET-UP (MM-2-6-1-PgDn)

DIAL MODE		PRINTER PARITY	
COMM MODE		PRINTER BAUD	
(DIRECT DIAL)	////////	MONITOR PORT	

Dial Mode: 0 = RS2-232 null, 1 = Hayes, 2 = UDS, 3 = 202 or MDM100
Comm Mode: 0 = LM SYS, 1-4 = MATS 1200, 2400, 4800, 9600 baud
Printer Parity: 0 = 7 bit no parity, 1 = 7 bit odd, 2 = 7 bit even, 3 = 7 bit space or 8 bit none
Printer Baud: 300, 1200, 2400, 4800, 9600
Monitor Port: 1 = RS-232A, 2 = RS-232B

PHONE NUMBERS (MM-2-6-2)

PRIMARY	
SECONDARY	

Special characters: P = pulse, T= Tone, comma = pause, W = Wait for DT
To insert special characters, hit decimal point, move cursor to desired character on display screen, then hit decimal again.

MODEM INITIALIZATION STRING(MM-2-6-2-PgDn)

Use left & right arrows to move to desired character. Use up/down arrows to scroll through alphabet and special characters.

SPECIAL FUNCTION CKT MAPPING (MM-2-6-3-PgDn, etc.)

FUNCT	1	2	3	4	5	6	7	8
CIRCUIT								
DELAY								

FUNCT	9	10	11	12	13	14	15	16
CIRCUIT								
DELAY								

FUNCT	17	18	19	20	21	22	23	24
CIRCUIT								
DELAY								

For system use. Function bits 1-24 issued from central via comm. Function bit is mapped to a clock circuit to initiate a specific action. Delay range: 0-9.9 or 127. Delay is from receipt of function bit to activation of ckt.

SYSTEM WIDE MAP SIGNAL ASSIGNMENTS (MM-2-6-4)

SIG1	SIG2	SIG3	SIG4	0 = Signal not used
				1-8 = ph/s 1-8, 9-12 = O/L A-D

The system wide map can support up to 4 signal colors as assigned.

TBC BACK-UP DELAY TIME (MM-2-6-5)

DELAY	0 -255 minutes. Determines delay period from
	lost carrier (lost comm) to when TBC takes over

NOTES

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REPORTS SET-UP

FUNCTION SCHEDULING (MM-2-7-1-PgDn, etc.)

FUNCT	UD1	UD2	UD3	UD4	UD5	UD6	UD7	UD8
MODE								

FUNCT	CLK	PWR	FRM	MMU	CHK	DET	RFL	MCE
MODE								

FUNCT	HPE	CYC	CRD	KEY	SYS	FLM	LPE	MOE
MODE								

Mode range: 0 = none, =1 - 3 = Sched A, B, C, 4 = request

VOLUME LOG SET-UP (MM-2-7-2)

NORM		For either: 0 = disable, 1, 5, 6, 10, 15, 30, or 60
ALT		= sampling period in minutes, 99 = by cycle

Alternate sampling period selected by clock ckt 136

DET's ENABLED FOR VOL LOGGING (MM-2-7-1-PgDn, etc.)

DET	1	2	3	4	5	6	7	8
MODE								

DET	9	10	11	12	13	14	15	16
MODE								

DET	17	18	19	20	21	22	23	24
MODE								

Mode = ON/OFF, ON = Det will log, OFF = No logging

MOE AND SPEED LOG SET-UP (MM-2-7-3)

NORM		For either: 0 = disable, 5, 6, 10, 15, 30, or 60
ALT		= sampling period in minutes
TRAP		0 - 255; Discard speeds above this value

Alternate sampling period selected by clock ckt 140

TRUE SPEED TRAP SET-UP (MM-2-7-3-PgDn)

SPEED TRAP	A	B	C	D
DETECTORS	9/10	11/12	13/14	15/16
DISTANCE				
UNITS				

Distance range: 0-255 units. Units: 0=Inches, 1=Feet, 2=Cent. 3=Decim.

COMPUTED SPEED DET SET-UP (MM-2-7-3-PgDn, etc.)

DET	1	2	3	4	5	6	7	8
TIME								

DET	9	10	11	12	13	14	15	16
TIME								

DET	17	18	19	20	21	22	23	24
TIME								

Time range; 0 - 255 hundredths of a second. Compute time based on ave veh at 30 MPH (50 KPH) over loop. For example, an average vehicle (16') would occupy a 6' x 6' loop for 44'/sec divided by (16'+6') = 50 hundredths.

MOE VOL/OCC DET ASSIGNMENTS (MM-2-7-3-PgDn, etc.)

DET	1	2	3	4	5	6	7	8
MOE PH								

DET	9	10	11	12	13	14	15	16
MOE PH								

DET	17	18	19	20	21	22	23	24
MOE PH								

MOE Phase range; 0 - 8. Assigns detectors to phases for MOE logging so that volume and occupancy counts can be tabulated on a per phase basis.

CALL IN DELAY SET-UP (MM-2-7-4)

SCHEDULE	A	B	C	VOLUME
DELAY TIME				

Delay range: 0- 255 minutes. Delays prevent repeated call-ins over a short period due to multiple events. By delaying, the unit will tend to collect data for a while then call it all in at once.

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TRANSIT PRIORITY

Note: special I/O must be configured for TP operation (see input mapping)

TRANSIT PRIORITY INPUT SET-UP

PHASES/MEMORY/DELAY (MM-2-8-1-1)

TP INPUT	1	2	3	4	5	6
PHASES						
DELAY						
MEMORY						

Phases = Priority phases, up to four phases per TP input
Delay = 0 - 255 secs, Memory = ON/OFF

INPUT TIMINGS (MM-2-8-1-2) Also see TP input mapping

TP INPUT	1	2	3	4	5	6	ALL
MAX WAIT							///////
MAX EXT							///////
MIN RSVC							

MAX WAIT = 0 - 255 secs = Maximum time unit will wait for TP ph
MAX EXT = 0 - 255 secs = Max time green can extend past Max or FO
MIN RSVC = 0 - 99 min = Min time allowed between successive operations on same TP input. ALL applies to any two successive TP inputs 1-6.

INPUT PRIORITIES (MM-2-8-1-3)

TP INPUT	1	2	3	4	5	6
PRIORITY						

Priority = 1-3, 1 = Lowest, 3 = Highest. Higher overrides lower

TP GROUP TIMINGS

GRP MAX TIMES (MM-2-8-2-1)

PHASE	1	2	3	4	5	6	7	8
GP1 MAX								
GP2 MAX								
GP3 MAX								

Range = 0 -255 secs. Set shorter than normal max or split time. Values determine the minimum length of green when phases are shortened to get to a TP Phase. Groups are selected by Cycle & Split to group assignment.

GRP WALK TIMES (MM-2-8-2-2)

PHASE	1	2	3	4	5	6	7	8
GP1 WLK								
GP2 WLK								
GP3 WLK								

Range = 0 -9.9 or 127 secs. Set shorter than normal walk time. Values determine the minimum length of walk when shortened to get to a TP Ph.

TRANSIT PRIORITY FREE MODE (MM-2-8-3)

MODE	0 = Use shortest of Max 1 or 2 and standard Walk times
	1-3 = Use Max and Walk time from groups 1-3

Determines how Phases will be shortened when unit is in free operation.

TRANSIT PRIORITY COORD OPTIONS

CYCLE & SPLIT TO MAX/WLK GROUPS 1-3 (MM-2-8-4-1)

CYCLE	1	2	3	4	5	6	7	8
SPLIT 1/2	/	/	/	/	/	/	/	/
SPLIT 3/4	/	/	/	/	/	/	/	/

Range 1-3. Example; under Cycle 1 in the split 1/2 row, the value “1/2” would assign group 1 times to C1S1 and group 2 times to C1S2.

PRE TP CYCLE LEADING LIMITS (MM-2-8-4-2)

PHASE	1	2	3	4	5	6	7	8
LIMIT								

Range: 0 = No limit, 1 - 255 secs = maximum time before force off phase is allowed to terminate when transitioning to TP phase.

POST TP MAX EXT’S UNTIL FIRST FORCE OFF (MM-2-8-4-3)

PHASE	1	2	3	4	5	6	7	8
MAX EXT								
AUT EXT								

Max Ext range = 0 -255 secs. Provides extension to max time after TP until 1st force off. Allows phases that may start early time out to their force off.

Aut Ext - ON/OFF. Automatically extends phase after TP until 1st force off.

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I/O CONFIGURE

_____ **Base Configuration Mode** (0 = TS1, 1-5 = Type 2 modes 1-5, 8 = Type 1)

PORT 1 BIU/MMU OPTIONS

BIU ENABLES (MM-4-1-1)

T/F BIU	1	2	3	4	5	6	7	8
////////////////								
DET BIU	9	10	11	12	13	14	15	16
////////////////								

ON/OFF; ON = BIU position enabled T/F= Terminal & Facilities (load sw's)

PORT 1 OPTIONS (MM-4-1-2)

PEER TO PEER		ON = Peer to Peer (other unit)
MMU DISABLE		ON = Port 1 disabled (TS1 mode)
TYPE 2 RUN AS TYPE 1		ON = BIU's instead of MSA, B. C

PHASE TO LOAD SWITCH (MMU CHAN) ASSIGN (MM-4-1-3)

PHASE	1	2	3	4	5	6	7	8
CHANNEL								

OVERLAP	A	B	C	D
CHANNEL				

PED	1	2	3	4	5	6	7	8
CHANNEL								

Range; 1-16. Assigns MMU channel 1-16 to each phase, O/L, Ped

PEER TO PEER POLLING ADDRESSES (MM-4-1-4)

NOTES

CUSTOM INPUT MAPPING (MM-4-2-3-PgDn, etc.)

VEH DETECTORS 1-8

INP FUNC	VD1	VD2	VD3	VD4	VD5	VD6	VD7	VD8
PIN #								
LOGIC								
PIN #								

VEH DETECTORS 9-16

INP FUNC	VD9	VD10	VD11	VD12	VD13	VD14	VD15	VD16
PIN #								
LOGIC								
PIN #								

VEH DETECTORS 17-24

INP FUNC	VD17	VD18	VD19	VD20	VD21	VD22	VD23	VD24
PIN #								
LOGIC								
PIN #								

VEH DETECTORS 25-32 (currently not supported, DO NOT PROGRAM)

INP FUNC	VD25	VD26	VD27	VD28	VD29	VD30	VD31	VD32
PIN #	0	0	0	0	0	0	0	0
LOGIC	OR	OR	OR	OR	OR	OR	OR	OR
PIN #	0	0	0	0	0	0	0	0

PED DETECTORS 1-8

INP FUNC	PED	PED	PED	PED	PED	PED	PED	PED
PIN #								
LOGIC								
PIN #								

PHASE HOLD 1-8

INP FUNC	HLD1	HLD2	HLD3	HLD4	HLD5	HLD6	HLD7	HLD8
PIN #								
LOGIC								
PIN #								

Note: Blanks = Standard default mode, make entries by exception only

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INPUT MAPPING CONTINUED....

VEH OMITS 1-8

INP FUNC	VOM1	VOM2	VOM3	VOM4	VOM5	VOM6	VOM7	VOM8
PIN #								
LOGIC								
PIN #								

PED OMIT1-8

INP FUNC	POM1	POM2	POM3	POM4	POM5	POM6	POM7	POM8
PIN #								
LOGIC								
PIN #								

PRE-EMPT 1-6

INP FUNC	PRE	PRE	PRE	PRE	PRE	PRE		
PIN #								
LOGIC								
PIN #								

Walk Rest, Ext min rec, SGO/Cond serv, Week program 10, Alt seq A-D

INP FUNC	WRM	MRCL	SQCS	WP10	ASQA	ASQB	ASQC	ASQD
PIN #								
LOGIC								
PIN #								

Man Control Enable, Int Adv., Ext. Start, Test A-C, Dim, Lamp disable (n/u)

INP FUNC	MCE	IADV	EXST	TSTA	TSTB	TSTC	DIM	LAMP
PIN #								
LOGIC								
PIN #								

Monitor status A-C, Monitor flash status, Local flash status, Flash mon1 & 2

INP FUNC	MONA	MONB	MONC	MON	LCFL	FLM1	FLM2	
PIN #								
LOGIC								
PIN #								

Timing Plan A-D (cyc2, cyc3, spl2, spl3), Offset 1-3 inputs, TBC on-line

INP FUNC	PLNA	PLNB	PLNC	PLND	OFF1	OFF2	OFF3	TBC
PIN #								
LOGIC								
PIN #								

Call to free, Sync inh, Call to sys, Clk sync, Int inh, Auto Flash, CNA 1 & 2

INP FUNC	CTF	SNCI	CSYS	TSNC	ITCI	AUTF	CNA1	CNA2
PIN #								
LOGIC								
PIN #								

Force off R1, R2, Inh max R1 R2, Call max 2 R1, R2, Omit red clear R1, R2

INP FUNC	FRC1	FRC2	IMX1	IMX2	MX21	MX22	ORC1	ORC2
PIN #								
LOGIC								
PIN #								

Ped recycle R1-R2, Red rest mode R1-R2, Stop time R1-R2, Coord ped rec

INP FUNC	PCY1	PCY2	RRM1	RRM2	STM1	STM2	CPR	
PIN #								
LOGIC								
PIN #								

User defined alarm inputs 1-8 (can be stored and/or called in via system)

INP FUNC	UDA1	UDA2	UDA3	UDA4	UDA5	UDA6	UDA7	UDA8
PIN #								
LOGIC								
PIN #								

SYSTEM ADDRESS INPUT FUNCTIONS

INP FUNC	ADR0	ADR1	ADR2	ADR3	ADR4	ADR5	ADR6	ADR7
PIN #								
LOGIC								
PIN #								

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INPUT MAPPING CONTINUED....

VD33-VD64 ARE NOT SUPPORTED, DO NOT PROGRAM

PRE-EMPT NO DELAY INPUTS

INP FUNC	PND1	PND2	PND3	PND4	PND5	PND6		
PIN #								
LOGIC								
PIN #								

TRANSIT PRIORITY REQUEST INPUTS 1-6, TRANSIT PRIORITY INHIBIT

INP FUNC	TPr1	TPr2	TPr3	TPr4	TPr5	TPr6	TPrI	
PIN #								
LOGIC								
PIN #								

TRANSIT PRIORITY CLEAR INPUTS 1-6

INP FUNC	TPC1	TPC2	TPC3	TPC4	TPC5	TPC6		
PIN #								
LOGIC								
PIN #								

TRANSIT PRIORITY PHASE 1-8 SHORTEN INHIBIT INPUTS 1-8

INP FUNC	TIP1	TIP2	TIP3	TIP4	TIP5	TIP6	TIP7	TIP8
PIN #								
LOGIC								
PIN #								

TRANSIT PRIORITY INPUT DEFINITIONS

TPr1-TPr6. These call Transit Priority for the assigned phases (assignment and timing in TP set-up programming). Once the TP phase has been achieved, it will hold until the input goes away or the TP maximum extend period times out.

TPrI. When activated, all Transit Priority inputs are inhibited (no TP allowed).

TPC1-TPC6. Each clears its corresponding call from memory (it also disables the request input when active). Typically used with two detector systems where the first is placed on the near side of the intersection using a TPr (request) input with memory set to on. The second is on the far side of the intersection and uses a TPC (clear call) input to clear the call once the vehicle is through the intersection.

TIP1-TIP8. When activated, Transit Priority can not shorten the corresponding phase if the phase is not the TP phase. The phase itself can be a TP phase.

OUTPUT MAPPING (MM-4-2-4-PgDn, etc.)

PHASE 1-8 RED, YELLOW GREEN OUTPUTS

	PH1	PH2	PH3	PH4	PH5	PH6	PH7	PH8
RED PIN #								
YEL PIN #								
GRN PIN #								

OVERLAP A-D RED, YELLOW GREEN OUTPUTS

	OLA	OLB	OLC	OLD				
RED PIN #								
YEL PIN #								
GRN PIN #								

PHASE 1-8 DON'T WALK, PED CLEAR, WALK OUTPUTS

	PH1	PH2	PH3	PH4	PH5	PH6	PH7	PH8
DW PIN #								
PCL PIN #								
WLK PIN #								

PHASE 1-8 CHECK, NEXT, ON OUTPUTS

	PH1	PH2	PH3	PH4	PH5	PH6	PH7	PH8
CHK PIN #								
NXT PIN #								
ON PIN #								

Time clk Plan A-D (cyc/spl), Offset 1-3, Aux 1-4, Hold out, sys out, sys call

FUNCT	PLNA	PLNB	PLNC	PLND	OFF1	OFF2	OFF3	FLC
PIN #								
FUNCT	AUX1	AUX2	AUX3	AUX4		HOLD	SYS	SYSC
PIN #								

PE1-6 out, Flash out, FL logic, Coded stat bits, Fast FL stat, Fast FL image

FUNCT	PE1	PE2	PE3	PE4	PE5	PE6	FL	FLO
PIN #								
FUNCT	CSA1	CSB1	CSC1	CSA2	CSB2	CSC2	FFL	FFLO
PIN #								

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OUTPUT MAPPING CONTINUED...

ADVANCE WARNING OUTPUT FUNCTIONS FOR PHASES & O/L's

FUNCT	ADW1	ADW2	ADW3	ADW4	ADW5	ADW6	ADW7	ADW8
PIN #								
FUNCT	ADWA	ADWB	ADWC	ADWD				
PIN #								

SPECIAL FUNCTION BIT 1-16 OUTPUTS Note: Activated remotely via sys

FUNCT	SF1	SF2	SF3	SF4	SF5	SF6	SF7	SF8
PIN #								
FUNCT	SF9	SF10	SF11	SF12	SF13	SF14	SF15	SF16
PIN #								

SPEC 17-24, Contrast bits, Backlight bit, CVM/Fault Monitor Inhibits

FUNCT	SF17	SF18	SF19	SF20	SF21	SF22	SF23	SF24
PIN #								
FUNCT	CNT0	CNT1	CNT2	CNT3	EL	CVMI	FMI	
PIN #								

DETECTOR SIMULATOR OUTPUT FUNCTIONS

FUNCT	DS01	DS02	DS03	DS04	DS05	DS06	DS07	DS08
PIN #								
FUNCT	DS09	DS10	DS11	DS12	DS13	DS14	DS15	DS16
PIN #								

PRE-EMPT ACKNOWLEDGE OUPTUTS 1-6

FUNCT	PEA1	PEA2	PEA3	PEA4	PEA5	PEA6		
PIN #								

CHANNEL 1-8 RED, YELLOW GREEN OUTPUTS

	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
RED CH #								
YEL CH #								
GRN CH #								

CHANNEL 9-16 RED, YELLOW GREEN OUTPUTS

	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
RED CH #								
YEL CH #								
GRN CH #								

INPUT FUNCTIONS DEFINTIONS

ABBREV	BRIEF COMMENT/DESCRIPTION
VD1-24	Vehicle Detector inputs 1-24 (see detectors/options)
VD25-32	Vehicle Detector inputs 25-32. Not currently supported by controller
PED1-8	Phase 1-8 pedestrian call inputs
HLD1-8	Holds Phases 1-8 at end of green (TDB pg 2-19)
VOM1-8	Omits (skips) phases 1-8
POM1-8	Omits peds for phases 1-8 (ph can still be served)
PRE1-6	Call pre-empt sequences 1-6 (allowing delay B4 PE)
WRM	Allows CNA phase to rest in walk after hold released
MRCL	Recall all phases, serves at least minimum green
SQCS	Phase stays gapped out/second service on left turns
WP10	Overrides normal week prog, goes to week prog. 10
ASQA-D	Alt sequence or "Lead/lag." A=reverse 1&2, B=3&4, C=5&6, D=7&8
MCE	Put calls on all phases, stops time except Yel & Red
IADV	Toggle advances to next interval, used w/MCE
EXST	Takes controller immediately to initialization interval
TSTA	Used in LMD controllers for DC remote flash (UCF)
TSTB	Programmable (controller options) Dim or Call free
TSTC	New TS2 test input, no defined function
DIM	Dimming by phase in color (see controller options)
LAMP	No function in LMD controllers due to LC displays
MONA-C	Receives 3 status bits from LSM or LNM monitors
MONF	Flash Receives MMU flash status from MMU
LCLF	Receives local flash status from switch, relay, etc.
FLM1/2	Monitors 2 flasher ckts, records alarm and/or calls in
PLNA-D	Implements timing plans 1-16 In cyc/spl terms; A=cyc2, B=Cyc3, etc.

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INPUT FUNCTIONS CONTINUED…..

ABBREV	BRIEF COMMENT/DESCRIPTION
OFF1-3	Offset inputs 1-3. Receives sync pulses from coord interconnect
TBC	TBC On-line . No function in LMD, use interconnect inhibit
CTF	Call to Free. Calls to free operation regardless of mode
SNCI	Sync Inhibit. Disables sync pulses on offset outputs
CSYS	Call to System operation input (interconnect mode)
TSNC	Time Clock Sync input. Resets clock to programmable time
ITCI	Interconnect Inhibit . Enables TBC (when programmed in auto mode)
AUTF	UCF flash. Cycles to flash (see INIT/FL). Same as remote flash
CNAI/2	Call to non-act 1 and 2 inputs Places prog'd ph's in CNA mode
FRC1/2	Force off R1-R2. Forces phase in ring to yellow if past min timings
IMX1/2	Inhibit Max inputs R1-R2. Allows phase in ring to extend indefinitely
MX21/2	Call to Max II R1-R2. Causes phase in ring to use Max II timings
ORC1/2	Omit Red Clear R1-R2.Causes phase in ring to skip red clear timing
PCY1/2	Ped Recycle inputs R1-R2. Allows phase in ring to recycle ped
RRM1/2	Red Rest Mode R1-R2. Ring rests in red if no calls (not last grn)
STM1/2	Stop Time inputs R1-R2. Causes all interval timers in ring to stop
CPR*	Coord Ped Recycle (see CPR note)
UDA1-8	User defined alarm inputs 1-8 Can be logged, called in by system
ADR0-7	System address bits 0-7. Wired in cabinet, sets system address
VD33-64	Vehicle Detectors 33-64. Not currently supported by controller
PND1-6	Same as PRE inputs but ignore delay B4 PE timing
TPr1-6	Transit Priority request inputs. Calls for TP phase
TPrI	Transit Priority Inhibit input. Disallows all Transit Priority operation
TPC1-6	Transit Priority Clear inputs. Clears TP call from memory
TIP1-8	TP Phase shorten inhibits. Disallows phase from being shortened by TP

OUTPUT FUNCTIONS

ABBREV	BRIEF COMMENT/DESCRIPTION
PLNA	Timing plan A output, driven by Clock ckt 1 (cyc 2) output
PLNB	Timing plan B output, driven by Clock ckt 2 (cyc 3) output
PLNC	Timing plan C output, driven by Clock ckt 6 (spl 2) output
PLND	Timing plan D output, driven by Clock ckt 7 (spl 3) output
OFF1	Offset 1 output, driven by Clock ckt 3 (Offset 1) output
OFF2	Offset 2 output, driven by lock ckt 4 (Offset 2) output
OFF3	Offset 3 output, driven by Clock ckt 5 (Offset 3) output

OUTPUT FUNCTIONS CONTINUED…

ABBREV	BRIEF COMMENT/DESCRIPTION
FLC	Flash call (command). Active when flash called for
AUX1-4	Clock Aux (general) outputs Clock ckts 9-12
HOLD**	Hold output. Active when coord ph hold applied (see note)
SYS	System output. Active when system achieved (F.O's active)
SYSC	System command. Active when system called for
PE1-6	Pre-empt 1-6 outputs. Activated by PE programming
FL	Flash Out. Active when Flash achieved
FLO	Flashing Logic Out 1 hz DC squarewave output
CSA1	Coded Status Bit A, ring 1 See TDB pg 2-26, 3-11
CSB1	Coded Status Bit B, ring 1 See TDB pg 2-26, 3-11
CSC1	Coded Status Bit C, ring 1 See TDB pg 2-26, 3-11
CSA2	Coded Status Bit A, ring 2 See TDB pg 2-26, 3-11
CSB2	Coded Status Bit B, ring 2 See TDB pg 2-26, 3-11
CSC2	Coded Status Bit C, ring 2 See TDB pg 2-26, 3-11
FFL	Fast Flash status output. Active when fast flashing
FFLO	Fast Flash logic output. Pulses at fast flash rate
ADW1-8	Advance warning ph 1-8 outs See TDB pg 2-9, 4-5
ADWA-D	Advance warning OL A-D outs See TDB pg 2-9, 4-5
SF1-24	Special Function outputs Allows MDM100 SF's to be mapped to pins
CNT0-3	Display contrast bits 0-3. Do not change these--will lose cont. control
EL	Display backlight control Do not change--will lose backlight control
CVMI	Controller Voltage Mon inhib. Active when software disables CVM
FMI	Fault Monitor inhibit Same as CVMI, but not active in planned (auto) FL
DS01-24	Detector simulator outputs. Allows outputs to be mapped to pins.
PEA1-6	Pre-empt acknowledge 1-6. Active upon receipt of PE call, even during delay before pre-empt period.

***CPR NOTE**: When WRM = OFF and Ped Recycle = ON, CNA coord phases will always go to Ped Clear upon the first permissive--regardless of demand. If there is no demand, the CNA phase remains in green and eventually recycles the ped. CPR determines when the ped gets recycled. When CPR input = OFF, the ped recycles immediately after CNA ped clear. When CPR input = ON the CNA phase rests in Green/Don't Walk and allows the ped to recycle only after all permissives have ended. Because the Coord Phase(s) remain green/Don't Walk during permissive periods, CPR allows more immediate response to conflicting demand.

**HOLD OUTPUT NOTE The LMD8000 had allowed an option to assign hold out to MSD pin 48 or MSA pin d (phase 2 check). In the LMD9200 these are equivalent to HOLD output I/O mapping codes 448 and 127 respectively. Be sure to zero out the normal function (such as assign 0 to phase 2 check) before assigning hold out to a pin.

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PEEK TRAFFIC SYSTEMS, INC.

LMD 9200 PROGRAMMING CHARTS

Comments, changes, identification of errors, recommendations for improvement and additions are strongly encouraged. please mail, fax, or email to:

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SECTION XII

MAINTENANCE

LMD CHECK-OUT

The LMD controller, if faulty, should be removed from the cabinet and replaced with a known good unit. When substituting with a replacement unit, it is generally easiest to remove the Information Memory Card (IMC) from the faulty unit and insert it into the replacement unit. This will automatically transfer the programmed data and real time into the new unit upon power-up.

Power On Self Test (POST) will reveal potential failures with hardware and software, however, to check for data failures, go to the Run Mode Menu/Fault Status to verify there are no failures. Also, it is recommended that the records of the controller data be kept in the shop as well as in the field.

INTERNAL DIAGNOSTICS

The LMD9000 has an internal diagnostic routine as part of the standard operating software. Activation and operation of the internal diagnostic routine is described in the "LMD9000 Diagnostic Test Specification", TDB 161, which can be ordered from your distributor or from TCT. Please note that the internal diagnostic routine is not intended as a field troubleshooting procedure, but as a shop test. A special cable is required and the outputs and indications do not operate normally. Also, once executed, the LMD9000 must be restarted to exit the diagnostic routine.

FOLD DOWN PANEL

To access the LMD circuitry, fold down the front panel after loosening the two top thumbscrews. This will expose all boards, which are fastened by retaining clips. The Information Memory Card (IMC) is the small board inserted perpendicularly into the control board. To remove it, bend back the retaining clip at the top and gently slide it off the post. The board is now free to remove from the edge connector. Remove any other boards in a similar manner, while removing any ribbon cables or internal harness connectors.

SOCKET MOUNTED OPERATING SOFTWARE PROMS

The LMD9000 PROMS can be replaced when a revision upgrade is required. The socket positions are labeled on the PROMs, be sure to place them in the correct position and right side up. Also, check to be sure the upgrade is compatible with your existing programmed data.

INTEGRATED CIRCUIT REMOVAL & REPLACEMENT

An IC is not a discrete component but a functional circuit (or circuits) within itself. Furthermore, since an IC cannot be repaired it is only necessary to determine:

(1) That the IC is defective, generally by replacement one known to be good.

(2) That the defect was not caused by some other circuit malfunction. If it has been shown definitely that an IC is defective it must be replaced.

Surface Mount Technology

The LMD controller predominantly uses surface mounted IC components. Although this technology provides benefits in reliability, size, and performance, it does require different techniques in removing and replacing these components. The following is a list of what is required as a minimum to repair surface mount equipment;

Manual Station

This work station is the minimum required and would consist of a well lighted work area, grounded to prevent static electricity damage to the electronic components, and a set of tools similar to the list below.

- Tweezers
- Small tip soldering iron
- Temperature indicating lacquer
- Braided solder wick
- Solder paste syringe dispenser
- RMA flux
- Hot air repair station
- Heat shields

Several sizes of tweezers will be required to handle the smallest packages and chip capacitors all the way up to the 84 pin PLCC (Plastic Leaded Chip Carrier). Some soldering irons have special de-soldering tips that can be used for almost all small SMC's in addition to standard soldering tips. Also, there are individual de-soldering tools that appear to be the equivalent of "hot tweezers" that are designed to remove a specific size of SMC.

Temperature indicating lacquers are useful for safe removal of a defective component. A temperature on the low side (184 ^{o}C) is preferable, as the body heats a little slower than the leads. The braided solder wick is a standard item sold by several electronic hobby shops.

Bench Repair

The major procedure needed in the field is the ability to remove and replace a defective component. The tools listed under the manual station will be necessary. The best procedure to follow for removal and replacement is listed below. Step 11 would be accomplished by using the repair station with due care to monitor the solder reflow, removing the heat immediately after the solder has achieved a thorough reflow. In an emergency situation, a component can be attached by using tweezers, soldering iron, and solder paste. Careful application of heat and solder is still the important issue. Clean-up can be achieved by using an aerosol spray can of appropriate solvent.

Procedure

1. Correctly identify the defective component.

2. Paint a small amount of temperature sensitive lacquer on the defective component.

3. Set up the repair station and adjust the temperature controls according to board size and component mass.

4. Place the board on the repair station, centering the component under the hot air outlet.

5. Place a heat shield over the adjacent components or place the vacuum collet on the defective component.

6. Begin applying heat.

7. When the temperature sensitive lacquer gives a positive indication, remove the unit with tweezers and remove hot air from board. With the semiautomatic station, the vacuum collet will lift the unit and redirect the hot air.

8. The footprint must now be cleaned of excess solder with a soldering iron and solder wick to achieve smooth, planar lands.

9. Use the solder syringe dispenser to put a proper and even amount of solder paste on each component land.

10. Place the component with care to get it correctly aligned.

11. Reflow and clean by using the reflow and clean-up equipment.

SCHEMATIC and ASSEMBLY DRAWINGS

Schematic drawings and sub-assembly drawings have been provided for all major boards and assemblies within the LMD9000 series unit.

Assembly Drawing Description

0807559 (shts 1-3) A/D LMD9200 Controller

0807610 (shts 1-3) A/D LMD9100 Controller *

Schematic Drawing Description

0807391 Power Supply Board

0807381 (shts 1 and 2) Control Board

0807494 (shts 1-4) Type 2 Input/Output Board

0807587 Type 1 Input/Output Board *

0807394 Aux Input/Output Board

0807581 TS-2 Communications Board

0807397 TS-1 Communications Board

0807590 Fiber-optic Communications Board *

Sub Assembly Description

0807393 S/A Power Supply Board

0807418-1 S/A Control Board

0807389 S/A EEPROM/RTC Board

0807496-X (shts 1 and 2) Type 2 Input/Output Board

0807589-X Type 1 Input/Output Board *

0807173-2 S/A Display Module

0807172 S/A Transformer Harness

0807396 S/A Aux Input/Output Board

0807583 S/A TS-2 Communications Board

0807399 S/A TS-1 Communications Board

0807592 S/A Fiber-optic Communications Board *

* drawings unavailable at time of printing

Parts Lists

Parts lists have been provided for most component parts including TCT's part number as well as the manufacturer's part number. Most are available from standard electronic supply houses, except for those specified as TCT only. For those listed by other manufacturer's please exercise caution when obtaining "substitute" or "equivalent" parts other than the part and manufacturer listed. Suffice it to say that all parts are not created equal. The design characteristics and performance of individual parts do make a difference, and we do choose specific parts from specific manufacturers for a reason. When in doubt, consult your distributor or TCT.

PARTS LIST POWER SUPPLY BOARD S/A 0807393

Reference Symbol	Description	Comp Mfr's Part Number	Part Number
Integrated Circuits			
RN1	RES. NETWORK-100K, 7 ISO	BOURNS 4114R-001-104	020A86-136
RN2	RES. NETWORK-10K, 8 ISO	BOURNS 4116R-001-103	020A87-112
U1,2	PULSE WIDTH MODULATION CKT.	MOTOROLA MC34060A	121H43-001
U3,4,5	QUAD CAOMPARATOR/BUFFER	MOTOROLA MC33302P	021K11-001
U6	VOLTAGE CONVERTER W/REG.	LINEAR TECH LT1054N8	121K18-001
Transistors			
Q1,6,11,14	TRANSISTOR-AMPLIFIER, NPN	MOTOROLA MPSA06	120E35-001
Q2,8,10	TRANSISTOR-AMPLIFIER, PNP	MOTOROLA MPSA56	120E34-001
Q3,9	TRANSISTOR-POWER	MOTOROLA MJE16004	120E43-001
Q4,7,12	TRANSISTOR-DARLINGTON	MOTOROLA MPSA28	120E33-001
Q5,13	TRANSISTOR-DARLINGTON	T.I. TIP120	120E54-001
Capacitors			
C1,2,8,13,15,17, 18,19,25,30,32,39	CAP. .1 ufd, 50V, 20%, CER	AVX SA305C104MAA	120C29-104
C3	CAP. 2700 ufd, 7.5V, -10+ 100%, AE	SPRAGUE 672D278H7R5FV5C	120C62-278
C4,5,10,11	CAP. .01 ufd, 100V, 10%, CERAMIC	AVX SA201C103KAA	020C25-103
C6,16,21,26,33	CAP. .1 ufd, 100V, 20%, CERAMIC	AVX SA401C104MAA	120C36-104
C7,14,20,22,27	CAP. 4.7 ufd, 20V, 10%, TANTALUM	MALLORY TAC475K020P02	120D95-475
C9,12,	CAP. 1000 pfd, 100V, 10%, CER.	AVX SA201A102KAA	020C25-102
C23,28,31	CAP. .27 ufd, 50V, 10%, TANT	SPRAGUE 173D274X9050U	020D96-274
C24,29	CAP. 820 ufd, 40V,-10+ 100%, AL.E.	SPRAGUE 672D827H040FV5C	120C65-827
C34	CAP. 17,000 ufd, 75V, -10+ 75%,	SPRAGUE 36DE173G075BC5L	120C72-179
C35,36	CAP. 1 ufd, 35V, 20%, TANTALUM	UNION CARB. T322B105M035AS	020D86-105
C37	CAP. 22 ufd, 20V, 10%, TANTALUM	UNION CARB. T322D226K020AS	120D95-226
C38	CAP. 470 ufd, 20V,-10+ 100%, AL.EL	SPRAGUE 672D477H020EK5C	120C69-477
Diodes			
CR1	DIODE - ZENER, 7.5V, 1W	1N4737A	020F28-4737
CR2,9	DIODE - RECTIFIER, 4A	MUR410	120W30-001
CR3,12	DIODE - ZENER, 33V, 1W	1N4752A	020F28-4752
CR4	DIODE - ZENER, 24V, 1W	1N4749A	020F28-4749
CR5,6,10,15,16, 18,22,23,25	DIODE - RECTIFIER, 1A	1N4005	120W35-4005
CR7,8,11	DIODE - SIGNAL	1N4148	120F07-001
CR13	DIODE - ZENER, 7.5 V, 5W	1N5343B	120F30-5343
CR14	DIODE - ZENER, 6.8V, 500mW	1N5235B	020F27-5235
CR17,20,21,24	DIODE - RECTIFIER, 5A	1N5625	020W49-001
CR19	DIODE - ZENER, 13V, 1W	1N4743A	120F28-4743
Inductors			
L2,3	INDUCTOR, 250uh	DALE IH-3 250 uh	120J30-001
L1	INDUCTOR, .33uh	DALE IM-4 .33 20%	120J25-001

Reference Symbol	Description	Comp Mfr's Part Number	Part Number
Resistors			
R1,10,30,35,38 58,66,72	RES. 3.9K, 1/4W, 5%, CARBON	--	020A01-102
R2,59	RES. .1 OHM, 1W, 5%, MET. OXIDE	--	120A59-340
R3,8,19,31,34, 36,45,46	RES. 220 OHM, 1/4W, 5%, CARBON	--	020A01-072
R4,7,15,18,67	RES. 33K, 1/4W, 5%, CARBON	--	020A01-124
R5,12,26,41	RES. 620 OHM, 1/4W, 5%, CARBON	--	020A01-083
R6,9	RES. 9.1K, 1/4W, 5% CARBON	--	020A01-111
R11,14	RES. 1M, 1/4W, 5%, CARBON	--	020A01-160
R13,25	RES. 39K, 1/4W, 5%, CARBON	--	020A01-083
R16,48	RES. 5.1 OHM, 1/4W, 5%, CARBON	--	020A01-033
R17,60	RES. 4.7K, 1/2W, 1%, CARBON	--	020A04-104
R20,32,43,55,57, 69,74	RES. 1K, 1/4W, 5%, CARBON	--	020A01-088
R21,24,33,37,42, 44,52,53,64,70,80	RES. 10K, 1/4W, 5%, CARBON	--	020A01-112
R22,23	RES. 68 OHM, 1/4W, 5%, CARBON	--	020A01-059
R27	RES. 2740 OHM, 1/2W, 1%, GTO	--	020A44-098
R28,79	RES. 732 OHM, 1/2W, 1%, GTO	--	020A44-272
R29,40,49,63	RES. 47K, 1/4W, 5%, CARBON	--	020A01-128
R39	RES. 62K, 1/4W, 5%, CARBON	--	020A01-131
R47,65,68,71	RES. 100K, 1/4W, 5%, CARBON	--	020A01-136
R50,56	RES. 240K, 1/4W, 5%, CARBON	--	020A01-145
R51	RES. 330K, 1/4W, 5%, CARBON	--	020A01-148
R54	RES. 30K, 1/4W, 5%, CARBON	--	020A01-123
R61,62	RES. 2.4OHM, 5W, 5%, WIRE WND	--	020A24-025
R73	RES. 12K, 1/4W, 5%, CARBON	--	020A01-114
R75	RES. 100 OHM, 1/4W, 5%, CARBON	--	020A01-064
R76	RES. 2.1K, 1/2W, 1%, GTO	--	020A44-275
R77,78	RES. 243 OHM, 1/2W, 1%, GTO	--	020A44-271
Miscellaneous			
F1,F2	FUSE - 1 AMP, SLO-BLO	LITTLEFUSE 313000 SERIES	020T41-100
F1,F2	FUSEHOLDER & CAP	LITLEFUSE 345-101	120V59-001
J2,J3	RECEPTACLE - 4 POSITION	AMP 640499-1	021R71-004
M0V1,2	VARISTOR	GE V150LA10A	020L21-001
Q3	HEAT SINK	THERMALLOY 6073PB-SE-1	020T30-001
Q9	HEAT SINK	THERMALLOY 6072BSE-3/1	120T08-001
Q3,9	INSULATOR	THERMALLOY 53-77-2	120T06-220
VR1	INVERTER	ENDICOTT RESEARCH LPS24-2-1	120E64-001
VR2,3	REGULATOR	NATIONAL LM317T	021K06-001
--	PRINTED CIRCUIT BOARD (only)	TCT ONLY	0807392-CM-1&2

PARTS LIST S/A, CONTROL BOARD 0807418-1

Reference Symbol	Description	Comp. Mfr's Part Number	Part Number
Integrated Circuits			
RN1,2	RESISTOR NETWORK, 10K	CTS of BERNE 767-161R10K	121E50-112
U1,2	OCTAL D-TYPE FLIP-FLOP	NATIONAL MM74HC574WM	121F30-001
U3	Z280 MICROPROCESSOR	ZILOG Z8028010VSC REV J	121F51-001
U4,20	HEX INVERTER	NATIONAL MM74HC04M	121F11-001
U5,21	TRIPLE 3-INPUT NOR GATE	NATIONAL MM74HC27M	121F12-001
U6,7,8	QUAD 2-INPUT OR GATE	NATIONAL MM74HC32M	121F14-001
U10	PLD PROGRAMMED	AMD-AMPAL16L8LJC/PGM7401	121F76-001
U11,19	8 INPUT NAND GATE	NATIONAL MM74HC30M	121F13-001
U12	12 STAGE BINARY COUNTER	NATIONAL MM74HC4040M	121F46-001
U13	QUAD ANALOG SWITCH	RCA CD74HC4066M	121F47-001
U14,15	3 TO 8 LINE DECODER	NATIONAL MM74HC138M	121F20-001
U16	DUAL MONOSTABLE VIBRATOR	NATIONAL MM74HC123AM	121F17-001
U17	OCTAL BUS TRANSCEIVER	NATIONAL MM74HC245AWM	121F26-001
U18	OCTAL BUS BUFFER	NATIONAL MM74HC244WM	121F25-001
U22,23,27,28	PROM, UNPROG, 64K X 8 BIT	ATMEL AT27C512R-20DC	121K65-001
U22,23,27,28	PROM SET, LMD9000	TCT ONLY	see drawing 0807559
U24,29	STATIC RAM, 8192 X 8 BIT	ATMEL AT3864L-15RC	121F77-001
Capacitors			
C1-10,18-21, 25,26,28,31,36	CAP. .1ufd, 50V, + 80%, -20% CER.	M.E. (MURATA-ERIE NORTH AM) GRM42-6Y5V104Z050BD	121C01-104
C23,24	CAP. 22 pfd, 50V, 5%, CERAMIC	M.E. GRM42-6CDG220J050BL	121C03-220
C17,22,27	CAP. .01ufd, 50V, 10%, CERAMIC	M.E. GRM42-6X7R103K50V	121C02-103
C29,30	CAP. 4.7 ufd, 20V, 10%, TANT.	MEPCO/CEN49MC475C020K0ASFT	121C25-475
Diodes			
CR1	DIODE 1N4005	AMPEREX BYD17J	121D50-4005
CR2	DIODE 1N4148	AMPEREX PMLL4148	121D01-4148
Resistors			
R1	RES, 120K, 1/4W, 5%, CARBON	KOA SPEER RM73B2BT124J	121E02-138
R2	RES, 5.6K, 1/4W, 5%, CARBON	KOA SPEER RM73B2BT562J	121E02-106
R3	RES, 10 OHM, 1/4W, 5%, CARBON	KOA SPEER RM73B2BT100J	121E02-040
R4	RES, 430 OHM. 1/4W, 5%, CARBON	KOA SPEER RM73B2BT431J	121E02-079
R5-8	RES, 2.7K, 1/4W, 5%, CARBON	KOA SPEER RM73B2BT272J	121E02-098
R16	RES, 10K, 1/4W, 5%, CARBON	KOA SPEER RM73B2BT103J	121E02-112
Miscellaneous			
J1	HEADER - DOUBLE ROW, 16 PIN	AMP 102973-8	120P33-016
J2, J3	HEADER - DOUBLE ROW, 40 PIN	AMP 2-102973-0	120P33-040
J6	CONNECTOR, EDGE, 36 POS.	AMP 1-530844-5	120R42-036
Y2	CRYSTAL - 19.6608 MHZ	M-TRON MPI 19.6608	120G02-009
U22,23,27,28	SOCKET - 28 PIN	AMP 641873-1	020V90-028
--	PRINTED CIRCUIT BOARD	TCT ONLY	0807382

PARTS LIST S/A, INFORMATION MEMORY CARD 0807389

Reference Symbol	Description	Comp. Mfr's Part Number	Part Number
Integrated Circuits			
U9	REAL TIME CLOCK	NATIONAL MM58274CV	121F60-001
U26,31	EEPROM, 64K CMOS	ATMEL AT28C64-20JC	121F78-001
U32	QUAD ANALOG SWITCH	RCA CD74HC4066M	121F47-001
U33,34	OCTAL D TYPE FLIP FLOP	NATIONAL MM74HC574WM	121F30-001
Capacitors			
C11,12,28,37,38	CAP. .1ufd, 50V, + 80/-20% CER.	M.E. GRM42-6Y5V104Z050BD	121C01-104
C15	CAP. 7-40 pfd, 250V, CERAMIC	JOHANSON 9614	020C30-001
C16	CAP. 22 pfd, 50V, 5%, CERAMIC	M.E. GRM42-6CDG220J050BL	121C03-220
C34,35	CAP. 4.7 ufd, 20V, 10%, TANT.	MEPCO/CEN49MC475C020K0ASFT	121C25-475
Diodes			
CR4	DIODE 1N4148	AMPEREX PMLL4148	121D01-4148
Resistors			
R9,10,11	RES, 2.7K, 1/4W, 5%, CARBON	KOA SPEER RM73B2BT272J	121E02-098
R14	RES, 10 OHM, 1/4W, 5%, CARBON	KOA SPEER RM73B2BT100J	121E02-040
R15	RES, 430 OHM. 1/4W, 5%, CARBON	KOA SPEER RM73B2BT431J	121E02-079
R17	RES, 10K, 1/4W, 5%, CARBON	KOA SPEER RM73B2BT103J	121E02-112
Miscellaneous			
B2	BATTERY - NICAD, 2.4V	GE 41B017AC01101	021G02-002
B2	BATTERY CLIP	KEYSTONE 92	111F50-001
Y1	CRYSTAL - 32,768 KHZ	STATEK CX-1V 32.768 KHZ A	020G03-001
--	PRINTED CIRCUIT BOARD	TCT ONLY	0807388

PARTS LIST S/A, LMD9200 (TS-2 Type 2) INPUT/OUTPUT BOARD 0807496-X

Reference Symbol	Description	Comp. Mfr's Part Number	Part Number
Integrated Circuits			
RN1,2,5,8,9, 14-18,22,23,25,28	RES. NETWORK, 10K COMMON	CTS of BERNE 767-161R10K	121E50-112
RN3,10,11,21	RES. NETWORK, 68K COMMON	CTS of BERNE 767-161R68K	121E50-132
RN4,7,12,13,19, 20,24,26,27	RES. NETWORK 220K ISO.	CTS of BERNE 767-161R220K	121E51-144
RN30	RES. NETWORK 220 OHM ISO.	CTS of BERNE 767-163R221G	121E51-072
U1-4	GATE ARRAY TCT7145	TCT ONLY	121F01-7145
U6	QUAD LINE RECEIVER	SIGNETICS MC1489AD	121F54-001
U7	OPERATIONAL AMPLIFIER	MOTOROLA MC1741CD	121F52-001
U8	QUAD LINE DRIVER	SIGNETICS MC1488D	121F53-001
U9-12	8 CH ANALOG MULTIPLEXER	RCA CD74HC4051M	121F45-001
U13-25,30	TRANSISTOR ARRAY	SPRAGUE ULN2003L	121F50-001
U26	QUAD 2-INPUT OR GATE	NATIONAL MM74HC32M	121F14-001
U27	HEX INVERTER	NATIONAL MM74HC04M	121F11-001
U28	OCTAL D-TYPE FLIP-FLOP	NATIONAL MM74HC374WM	121F28-001
U29,31	3 TO 8 LINE DECODER	NATIONAL MM74HC138M	121F20-001
U32-34	OCTAL BUS BUFFER	NATIONAL MM74HC244WM	121F25-001
Capacitors			
C1-39,41-51 53-76,78-92	CAP. 0.1uf, 50V, + 80 -20% CER.	M.E. GRM42-6Y5V104Z050BD	121C01-104
C40,93	CAP. 4.7uf, 20V, 10% TANT.	MEPCO/CEN49MC475C020K0ASFT	121C25-475
C77	CAP. .01uf, 50V, 10%, CER.	M.E. GRM42-6X7R103K50V	121C02-103
Diodes			
CR2	DIODE 1N4005	AMPEREX BYD17J	121D50-4005
CR3	DIODE - ZENER 1N4752A	THOMSON BZM 85 C 33	121D25-4752
CR4-7	DIODE IN4148	AMPEREX PMLL4148	121D01-4148
Resistors			
R1	RES. 8.66K, 1/4, 1%	KOA SPEER RK73H2B-F8.66K	121E06-341
R2	RES. 17.4K, 1/4W, 1%	KOA SPEER RK73H2B-F17.4K	121E06-342
R3	RES. 34K, 1/4W, 1%	KOA SPEER RK73H2B-F34.0K	121E06-328
R4	RES. 68.1K, 1/4W, 1%	KOA SPEER RK73H2B-F68.1K	121E06-343
R5	RES. 10K, 1/4W, 1%	KOA SPEER RK73H2B-F10.0K	121E06-112
R6	RES. 3.01K, 1/4W, 1%	KOA SPEER RK73H2B-F3.01K	121E06-277
R7,8,15,16,40-49	RES. 68K, 1/4W, 5%	KOA SPEER RM73B2BT683J	121E02-132
R9-13,21	RES. 1K, 1/4W, 5%	KOA SPEER RM73B2BT102J	121E02-088
R14,17-20,22,24	RES. 10K, 1/4W, 5%	KOA SPEER RM73B2BT103J	121E02-112
R23,25	RES. 220K, 1/4W, 5%	KOA SPEER RM73B2BT224J	121E02-144
R29-32	RES. 220 OHM, 1/4W, 5%	KOA SPEER RM73B2BT220J	121E02-072
Miscellaneous			
J1	CONNECTOR-EDGE POS. 36	AMP 1-530844-4	120R42-036
J2	CONNECTOR POS. 40	AMP 86418-2	020R29-040
J3	HEADER-RT ANGLE POS. 12	AMP 1-87233-2	120P35-012
J4	CONNECTOR-D-TYPE POS. 25	AMP 745187-8	120R57-025D
J5	CONNECTOR, EDGE, 90°	SULLINS EZM22DTAS	120R77-044

Continued

PARTS LIST S/A, LMD9200 (TS-2 Type 2) INPUT/OUTPUT BOARD 0807496-X

Reference Symbol	Description	Comp. Mfr's Part Number	Part Number
Miscellaneous (continued)			
MSA	CONNECTOR POS. 55	ITT CANNON KPT 45528-415 SPCL	120R70-055
MSB	CONNECTOR POS. 55	ITT CANNON KPT 45528-428 SPCL	120R69-055
MSC	CONNECTOR POS. 61	ITT CANNON KPT 45528-268 SPCL	120R71-061
--	PRINTED CIRCUIT BOARD (only)	TCT ONLY	0807495

PARTS LIST S/A, LMD9100 (TS-2 Type 1) INPUT/OUTPUT BOARD 0807589-X

Reference Symbol	Description	Comp. Mfr's Part Number	Part Number
Integrated Circuits			
RN1,2,4	RES. NETWORK, 10K COMMON	CTS of BERNE 767-161R10K	121E50-112
RN3	RES. NETWORK 220 OHM ISO.	CTS of BERNE 767-163R221G	121E51-072
U1	GATE ARRAY TCT7145	TCT ONLY	121F01-7145
U2	QUAD LINE RECEIVER	SIGNETICS MC1489AD	121F54-001
U3	QUAD LINE DRIVER	SIGNETICS MC1488D	121F53-001
U4	HEX INVERTER	NATIONAL MM74HC04M	121F11-001
U5	TRANSISTOR ARRAY	SPRAGUE ULN2003L	121F50-001
U6	OPERATIONAL AMPLIFIER	MOTOROLA MC1741CD	121F52-001
U7	OCTAL D-TYPE FLIP-FLOP	NATIONAL MM74HC574WM	121F30-001
U8,10,12,13,18	3 TO 8 LINE DECODER	NATIONAL MM74HC138M	121F20-001
U9	QUAD 2-INPUT OR GATE	NATIONAL MM74HC32M	121F14-001
U11,14,16,17	DUAL D-TYPE F/F W/CLEAR	T.I. SN74HC74D	121H99-002
U15	OCTAL BUS BUFFER	NATIONAL MM74HC244WM	121F25-001
Capacitors			
C1-8,10-19,21	CAP. 0.1uf, 50V, + 80 -20% CER.	M.E. GRM42-6Y5V104Z050BD	121C01-104
C9	CAP. 0.01uf, 50V, + 80 -20% CER.	M.E. GRM42-602X7R102K050BD	121C02-102
C11,20	CAP. 4.7uf, 20V, 10% TANT.	MEPCO/CEN49MC475C020K0ASFT	121C25-475
Diodes			
CR1	DIODE - ZENER 1N4752A	THOMSON BZM 85 C 33	121D25-4752
CR3,4	DIODE IN4148	AMPEREX PMLL4148	121D01-4148
CR5	DIODE 1N4005	AMPEREX BYD17J	121D50-4005
Resistors			
R1,15-18	RES. 1K, 1/4W, 5%	KOA SPEER RM73B2BT102J	121E02-088
R3,5,19	RES. 10K, 1/4W, 5%	KOA SPEER RM73B2BT103J	121E02-112
R6	RES. 68.1K, 1/4W, 1%	KOA SPEER RK73H2B-F68.1K	121E06-343
R7	RES. 34K, 1/4W, 1%	KOA SPEER RK73H2B-F34.0K	121E06-328
R8	RES. 17.4K, 1/4W, 1%	KOA SPEER RK73H2B-F17.4K	121E06-342
R9	RES. 8.66K, 1/4, 1%	KOA SPEER RK73H2B-F8.66K	121E06-341
R10	RES. 3.01K, 1/4W, 1%	KOA SPEER RK73H2B-F3.01K	121E06-277
R11-14	RES. 220 OHM, 1/4W, 5%	KOA SPEER RM73B2BT220J	121E02-072
Miscellaneous			
J1	CONNECTOR-EDGE POS. 36	AMP 1-530844-4	120R42-036
J2	CONNECTOR POS. 40	AMP 86418-2	020R29-040
J3	HEADER-RT ANGLE POS. 12	AMP 1-87233-2	120P35-012
J4	CONNECTOR-D-TYPE POS. 25	AMP 745187-8	120R57-025D
MSA	CONNECTOR POS. 11	ITT CANNON MS3102E18-1P	020R49-001
–	ADAPTER PLATE (MSA)	TCT ONLY	0807583
–	LATCHING BLOCKS	AMP 745286-2	111N20-001
–	PRINTED CIRCUIT BOARD (only)	TCT ONLY	0807588

PARTS LIST S/A, DISPLAY MODULE 0807173-2

Reference Symbol	Description	Comp Mfr's Part Number	Part Number
Miscellaneous			
DISPLAY	LCD MODULE	DENSITRON LM2457B4C40CTH	120T64-001
DISP CONN.	HEADER, DOUBLE ROW - 16 PIN	AMP 102973-8	120P33-016
--	CONTACT, SOCKET	AMP 350665-1	020X95-001
--	HOUSING, CONNECTOR -2 POS.	AMP 1-640517-0	121P71-002

PARTS LIST S/A, TRANSFORMER HARNESS 0807172

Reference Symbol	Description	Comp Mfr's Part Number	Part Number
Miscellaneous			
T1	TRANSFORMER	EX-QUAL 111-1-017A	120H50-001
--	CONTACT, SOCKET	AMP 350665-1	020X95-001
--	CONNECTOR HOUSING	AMP 1-640519-0	021P71-004

PARTS LIST S/A, AUX I/O BOARD 0807396

Reference Symbol	Description	Comp. Mfr's part number	Part Number
Integrated Circuits			
RN1	RES. NET., 330K, 8 ISO. DIP	CTS of BERNE 767-163R330K	121E51-148
RN2,5,8, & 9	RES. NET., 220K, 8 ISO. DIP	CTS of BERNE 767-163R220K	121E51-144
RN3,6 & 10	RES. NET., 10K, 15 COM. DIP	CTS of BERNE 767-161R10K	121E50-112
RN4 & 7	RES. NET., 68K, 15 COM. DIP	CTS of BERNE 767-161R68K	121E50-132
RN11	RES. NET., 220, 8 ISO. DIP	CTS of BERNE 767-163R221G	121E51-072
U1 & 2	GATE ARRAY (CUSTOM) TCT7145	TCT ONLY	121F01-7145
U3	TRI-STATE OCTAL D-TYPE F/F	NATIONAL MM74HC574WM	121F30-001
U4	3- TO 8- LINE DECODER	NATIONAL MM74HC138M	121F20-001
U5	QUAD 2-INPUT NAND GATE	NATIONAL MM74HC00M	121F10-001
U6-8	DARLINGTON TRANS. ARRAY	SPRAGUE ULN2003L	121F50-001
U9-13	PHOTOTRANSISTOR, OPTO-ISO.	FAIRCHILD MCT6	120E71-001
Capacitors			
C1	CAP. 4.7 ufd, 20V, TANT	MEPCO/CEN49MC475C020K0ASFT	121C25-475
C2-7, 17-47,49-50	CAP. 0.1 ufd, 50V, CER.	M.E. GRM42-6Y5V104Z050BD	121C01-104
C8-16	CAP. 0.33 ufd, 50V, TANT	MEPCO/ELECT49MC334A035K0AS	121C26-334
C48	CAP. 0.001 ufd, 50V, CER.	M.E. GRM42-602X7R102K050BD	121C02-102
Diodes			
CR1, 4-12	DIODE, 1W, 1N4005	AMPEREX BYD17J	121D50-4005
CR2	DIODE-ZENER, 1W, 33V.	THOMSON BZM 85 C 33	121D25-4752
CR13	DIODE-ZENER, 1W, 82V.	THOMSON BZM 85 C 82	121D25-4762
Resistors			
R1-9	RES. 20K, 1/2W, + /-5% CARBON	--	020A04-119
R10, 12-25	RES. 10K, 1/4W, + /-5% CARBON	KOA SPEER RM73B2BT103J	121E02-112
R11	RES. 68K, 1/4W, + /-5% CARBON	KOA SPEER RM73B2BT683J	121E02-132
R26	RES. 330K, 1/4W, + /-5% CARBON	KOA SPEER RM73B2BT334J	121E02-148
R27-30, 32	RES. 220, 1/4W, + /-5% CARBON	KOA SPEER RM73B2BT220J	121E02-072
R31	RES. 10, 1/4W, + /-5% CARBON	KOA SPEER RM73B2BT100J	121E02-040
Miscellaneous			
--	MSD RECEPTACLE, 63 PIN	AMP 206455-2	021R61-001
--	CONNNECTOR PCB TYPE, 40 PIN	AMP 86418-2	020R29-040
--	PRINTED CIRCUIT BOARD	TCT ONLY	0807395

PARTS LIST TS-2 COMMUNICATIONS BOARD (with SDLC) S/A 0807583

Reference Symbol	Description	Comp Mfr's Part Number	Part Number
Integrated Circuits			
RN1	RES. NETWORK-10K, 15 COM	CTS of BERNE 767-161-R10K	121E50-112
RN2,4	RES. NETWORK-220K, 8 ISO	CTS of BERNE 767-163-R224G	121E51-144
RN3	RES. NETWORK-68K, 15 COM	CTS of BERNE 767-161-R68K	121E50-132
U1	OPERATIONAL AMPLIFIER	RAYTHEON RC4559M	121J84-002
U2	FSK MODEM	AMD AM7911JC	121K36-002
U3,4,9	OCTAL D-TYPE FLIP/FLOP	T.I. SN74HC574DW	121F30-001
U5	SCC SERIAL COM. CONTR.	ZILOG Z80C3008VSC	121J19-002
U6	QUAD LINE DRIVER	MOTOROLA MC75174BDW	121F56-001
U7	QUAD LINE RECEIVER	MOTOROLA SN75175D	121F57-001
U8,10	DECODER 3 TO 8 LINE	NATIONAL MM74HC138M	121F20-001
U11	DUAL D-TYPE F/F W/CLEAR	T.I. SN74HC74D	121H99-002
Transistors			
Q1,3	TRANSISTOR	MOTOROLA MMBTA06L	120E35-002
Q2	TRANSISTOR	MOTOROLA MMBTA56L	120E34-002
Capacitors			
C1,3	CAP. 2.2 ufd, 20V,10% TANT.	MEPCO 49MC225B020KOASFT	121C25-225
C2	CAP. 2200 pfd, 50V, 10% CER.	MURATA GRM42-6X7R222K050B	121C03-222
C4-26,28,30 32,34,35	CAP. 0.1 ufd , 50V, 20% CER.	MURATA GRM42-6Y5V104Z050BD	121C01-104
C27,33	CAP. 22 ufd , 16V , 10% TANT.	MEPCO 49MC226D016KOASFT	121C25-226
C29,31,36	CAP. 4.7 ufd, 20V , 10% TANT.	MEPCO 49MC475C020KOASFT	121C25-475
Diodes			
CR1, 2	DIODE - ZENER, 9.1V	PHILIPS BZV55C9V1	121D27-5239
CR3, 4	DIODE - ZENER, 4.7V	PHILIPS BZV55C4V7	121D27-5230
CR5	DIODE - ZENER, 5.1V	PHILIPS BZV55C5V1	121D27-5231
CR6	DIODE - ZENER, 12V	PHILIPS BZD27C12	121D25-4742
CR7	DIODE - RECTIFIER	AMPEREX BYD17J	121D50-4005
CR8	DIODE - SIGNAL	AMPEREX PMLL4148	121D01-4148
Resistors			
R1,20	RES. 240, 1/4W, + /-5% CARBON	KOA SPEER RM73B3AT241J	121E07-073
R2,10	RES. 560, 1/4W, + /-5% CARBON	KOA SPEER RM73B2BT561J	121E02-082
R3,4,7,11	RES. 22K, 1/4W, + /-5% CARBON	KOA SPEER RM73B2BT223J	121E02-120
R5	RES. 9.1K, 1/4W, + /-5% CARBON	KOA SPEER RM73B2BT912J	121E02-111
R8	RES. 62, 1/4W, + /-5% CARBON	KOA SPEER RM73B2BT620J	121E02-059
R9	RES. 620, 1/4W, + /-5% CARBON	KOA SPEER RM73B2BT621J	121E02-083
R12	RES. 100K , 1/4W , + /-5% CARBON	KOA SPEER RM73B2BT104J	121E02-136
R13	RES. 820 , 1/4W , + /-5% CARBON	KOA SPEER RM73B2BT821J	121E02-086
R14,18,24-26	RES. 10K, 1/4W, + /-5% CARBON	KOA SPEER RM73B2BT103J	121E02-112
R15	RES. 2.2K, 1/4W, + /-5% CARBON	KOA SPEER RM73B2BT222J	121E02-096
R16	RES. 3.3K, 1/4W, + /-5% CARBON	KOA SPEER RM73B2BT332J	121E02-100
R17	RES. 5.6K, 1/4W, + /-5% CARBON	KOA SPEER RM73B2BT562J	121E02-106

(continued)

Reference Symbol	Description	Comp Mfr's Part Number	Part Number
Resistors (continued)			
R19	RES. 24K, 1/4W, + /-5% CARBON	KOA SPEER RM73B2BT243J	121E02-121
R21,27	RES. 120, 1/2W, + /-5% CARBON	KOA SPEER RM73B2H121J	121E04-066
R23	RES. 1.2K, 1/4W, + /-5% CARBON	KOA SPEER RM73B2BT122J	121E02-090
R28	RES. 3.9K, 1/4W, + /-5% CARBON	KOA SPEER RM73B2BT392J	121E02-102
Miscellaneous			
J1	CONNECTOR - D - TYPE 9 POS.	AMP 205204-1	121P94-009D
J2,13	CONNECTOR - D - TYPE 15 POS.	AMP 745185-6	120R57-015D
J6	HEADER-D/ROW 12 POS.	AMP 87227-6	120P33-012
J7	HEADER SINGLE ROW 3 POS.	AMP 87224-3	120P34-001
J12	EDGE CONNECTOR , 90°, 36 POS.	SULLINS EZC18DTAS	120R76-036
T1,2	TRANSFORMER	TRW/UTC TC-SSO-33	020H71-002
--	PRINTED CIRCUIT BOARD (only)	TCT ONLY	0807582
--	LATCHING BLOCKS	AMP 745286-2	111N20-001

PARTS LIST TS-1 (WITHOUT SDLC) COMMUNICATIONS BOARD S/A 0807399

Reference Symbol	Description	Comp Mfr's Part Number	Part Number
Integrated Circuits			
RN1,5	RES. NETWORK-10K, 15 COM	CTS of BERNE 761-1-R10K	20A82-112
RN2,4	RES. NETWORK-220K, 10 ISO	CTS of BERNE 761-3-R220K	20A87-144
RN3	RES. NETWORK-68K, 15 COM	CTS of BERNE 761-1-R68K	20A82-132
U1	OPERATIONAL AMPLIFIER	RAYTHEON RV4559NB	121J84-001
U2	FSK MODEM	AMD AM7911PC	121K36-001
U3,4,7	OCTAL D-TYPE FLIP/FLOP	T.I. SN74HC574	121J09-001
U5,8	DECODER 3 TO 8 LINE	NATIONAL MM74HC138N	121J06-001
U9	DUAL D-TYPE F/F W/CLEAR	NATIONAL MM74HC74N	121H99-001
U10	SCC SERIAL COM. CONTR.	ZILOG Z803006PSC	121J19-011
U11	QUAD LINE DRIVER	SIGNETICS MC1488N	121J96-001
U12	QUAD LINE RECEIVER	T.I. MC1489N	121J97-001
Transistors			
Q1,3	TRANSISTOR	MOTOROLA MPAS06	120E35-001
Q2	TRANSISTOR	MOTOROLA MPSA56	120E34-001
Capacitors			
C1,3	CAP. 2.2 ufd, 35V,10% TANT.	UNION CARBIDE T322 SERIES	120C35-225
C2	CAP. 2200 pfd, 100V, 10% CER.	CORNING CAC03COG222K050A	120C37-222
C4-21,23-26,28 32,34,37	CAP. 0.1 ufd , 50V, 20% CER.	CORNING CAC04X7R104M050A	120C29-104
C27,33	CAP. 22 ufd , 20V , 10% TANT.	UNION CARB. T322D226K020AS	120D95-226
C31,36	CAP. 4.7 ufd, 20V , 10% TANT.	MALLORY TAC475K020P02	120D95-475
Diodes			
CR1, 2	DIODE - ZENER, 9.1V	ITT SEMICONDUCTOR 1N5239B	020F27-5239
CR3, 4	DIODE - ZENER, 4.7V	ITT SEMICONDUCTOR 1N5230B	020F27-5230
CR5	DIODE - ZENER, 5.1V	ITT SEMICONDUCTOR 1N5231B	020F27-5231
CR6	DIODE - ZENER, 12V	FAIRCHILD 1N4742A	120F28-4742
CR7	DIODE - RECTIFIER	GENERAL INSTRUMENTS 1N4005	120W35-4005
Resistors			
R1	RES. 240 OHM, 1W, 5%	--	20A06-073
R2,10	RES. 560 OHM ,1/4W, 5%	--	20A01-082
R3,4,7,11	RES. 22K , 1/4W, 5%	--	20A01-120
R5	RES. 9.1K , 1/4W, 5%	--	20A01-111
R8	RES. 62 OHM, 1/4W , 5%	--	20A01-059
R9	RES. 620 , 1/4W , 5%	--	20A01-083
R12	RES. 100K , 1/4W , 5%	--	20A01-136
R13	RES. 820 , 1/4W , 5%	--	20A01-086
R14,18,24,25	RES. 10K , 1/4W , 5%	--	20A01-112
R15	RES. 2.2K , 1/4W , 5%	--	20A01-096
R16	RES. 3.3K , 1/4W , 5%	--	20A01-100
R17	RES. 5.6K , 1/4W , 5%	--	20A01-106
R19	RES. 24K , 1/4W , 5%	--	20A01-121
R20	RES. 240 OHM , 1/2W , 5%	--	20A04-073
R23	RES.1.2K , 1/4W , 5%	--	20A01-090
R26	RES.3.9K , 1/4W , 5%	--	20A01-102

Reference Symbol	Description	Comp Mfr's Part Number	Part Number
Miscellaneous			
J1	CONNECTOR - D - TYPE 9 POS.	AMP 745183-5	120R57-009D
J2	CONNECTOR - D - TYPE 15 POS.	AMP 745185-6	120R57-015D
J4,7-11,13,14	JUMPER-WIRE INSULATED	VESTAL IN1057	20Z89-001
J5	HEADER SINGLE ROW 3 POS.	AMP 87224-3	120P34-001
J6	HEADER-D/ROW 12 POS.	AMP 87227-6	120P33-012
J12	EDGE CONNECTOR , 90°, 36 POS.	SULLINS EZC18DTAS	120R76-036
J15	CONNECTOR, D TYPE, 25 POS.	AMP 745187-6	120R57-025D
T1,2	TRANSFORMER	TRW/UTC TC-SSO-33	20H71-002
--	PRINTED CIRCUIT BOARD (only)	TCT ONLY	087398

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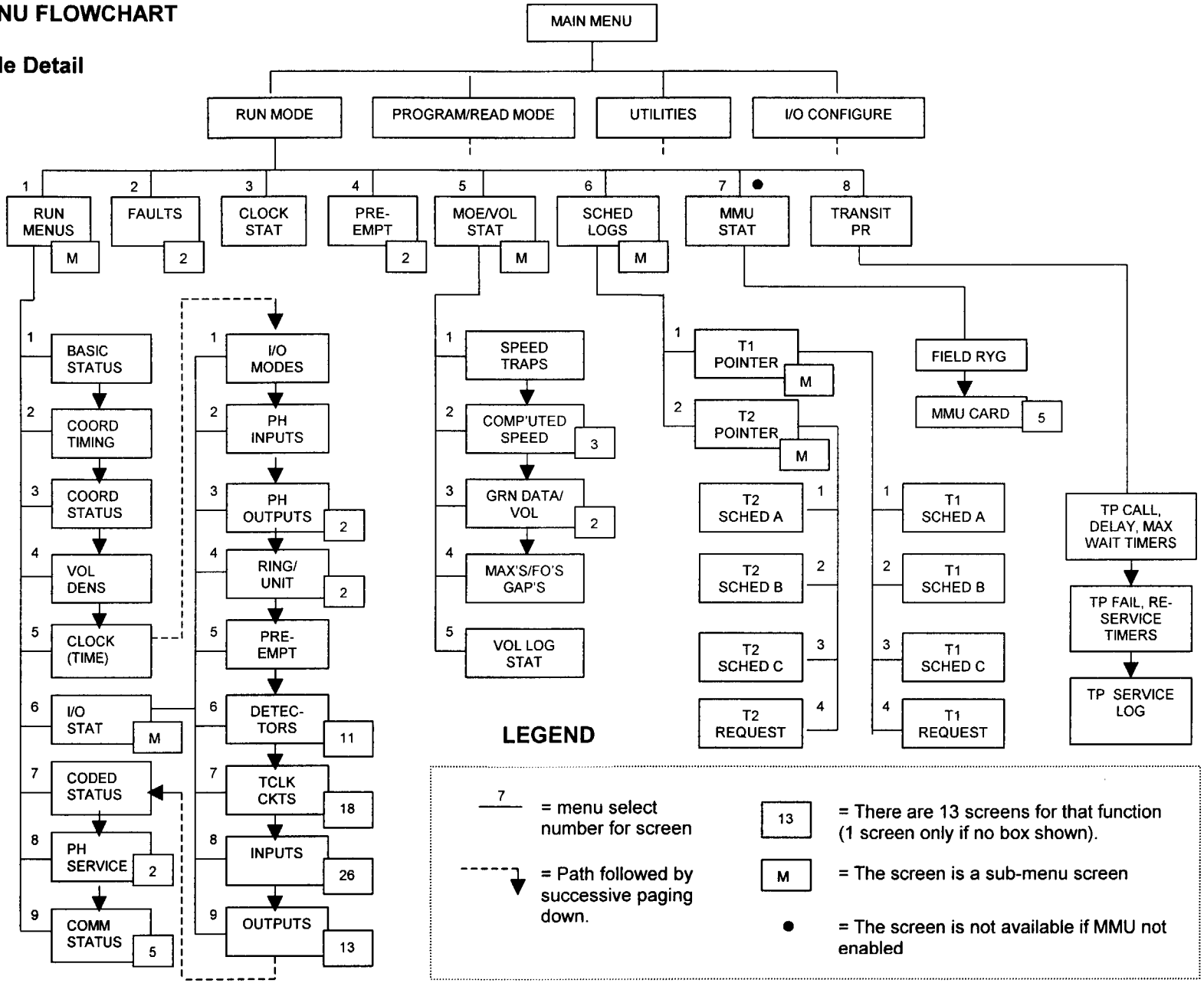
Run Mode Detail



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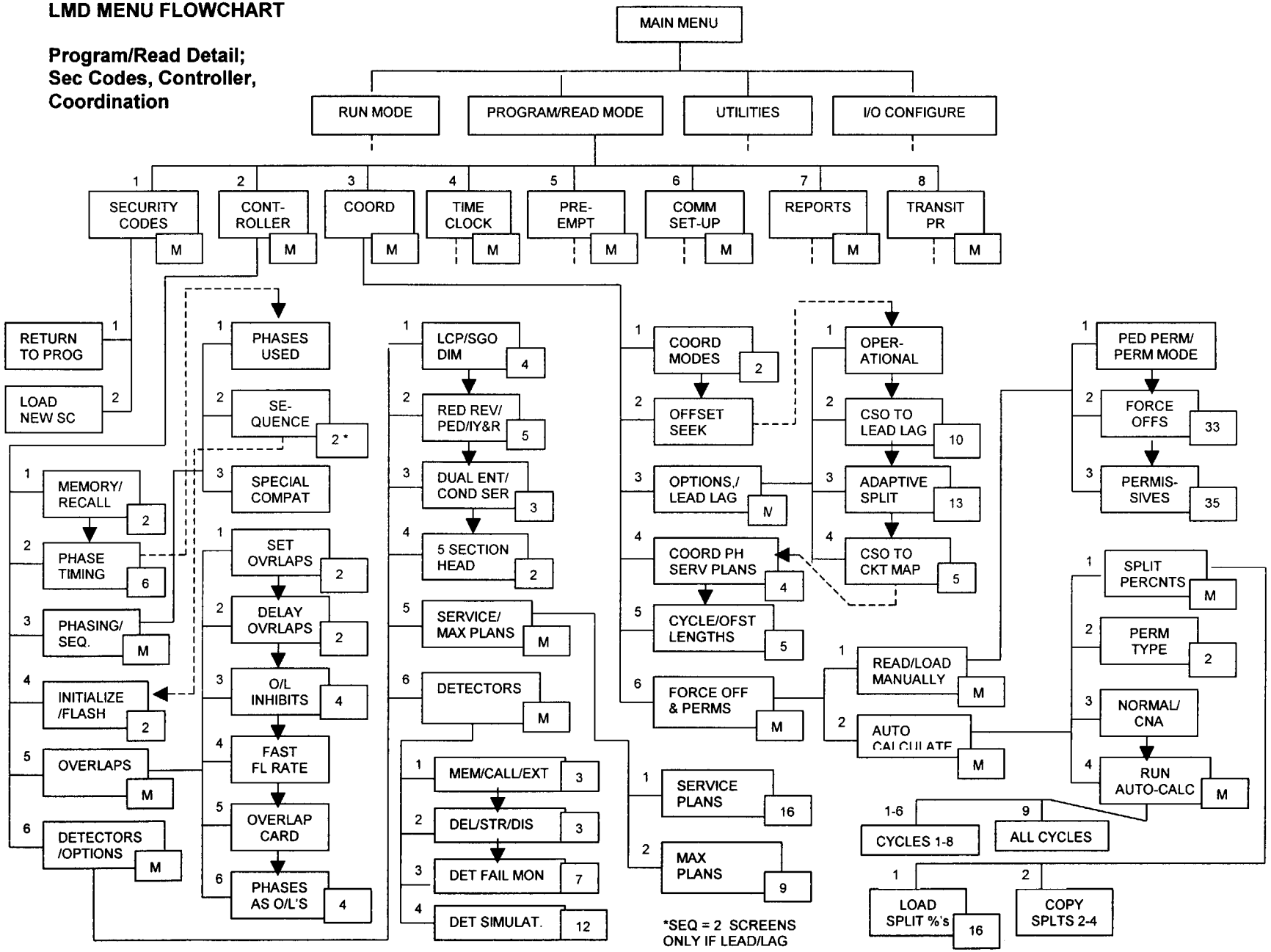
Program/Read Detail; Sec Codes, Controller, Coordination



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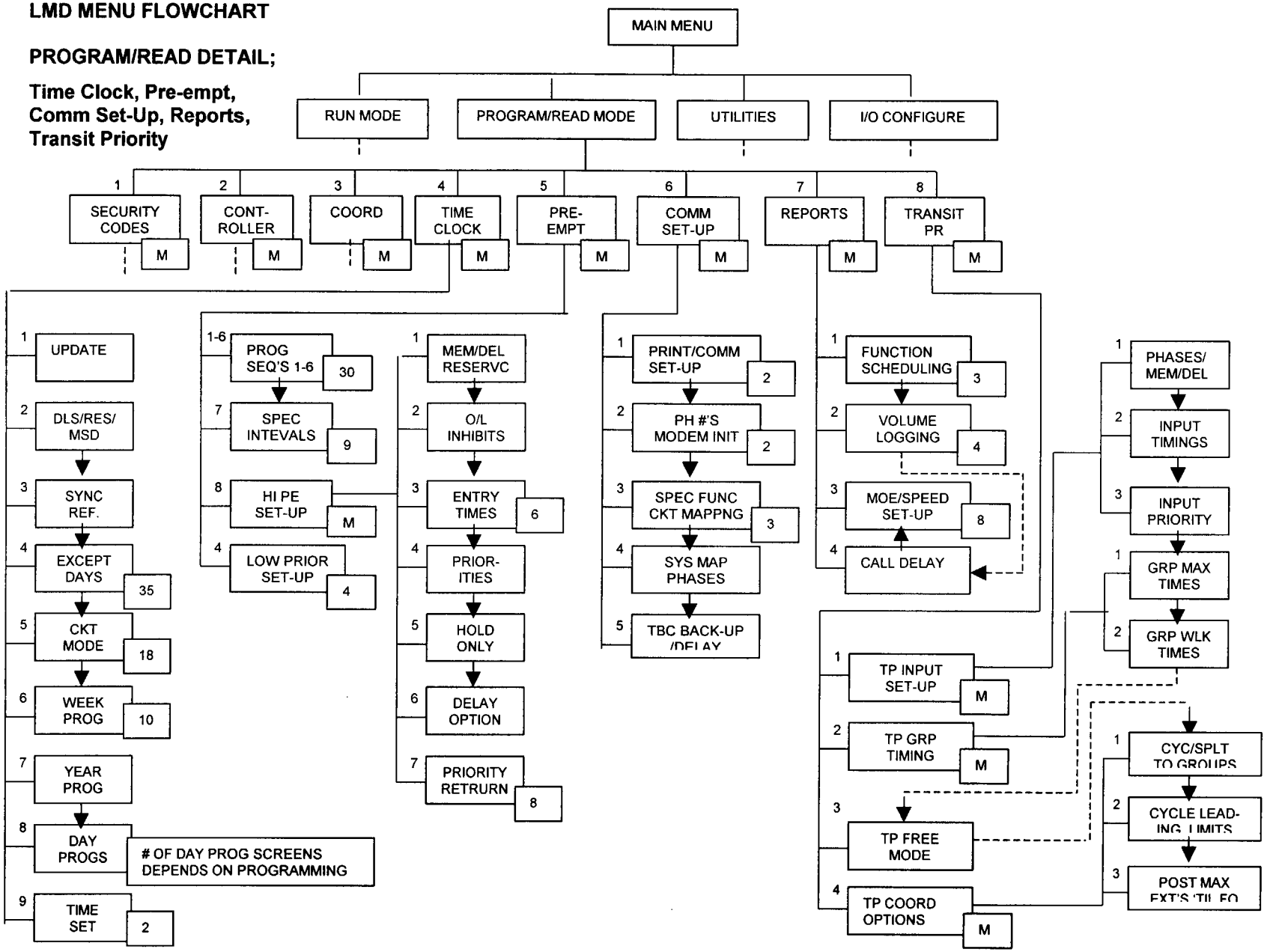
PROGRAM/READ DETAIL;

Time Clock, Pre-empt, Comm Set-Up, Reports, Transit Priority



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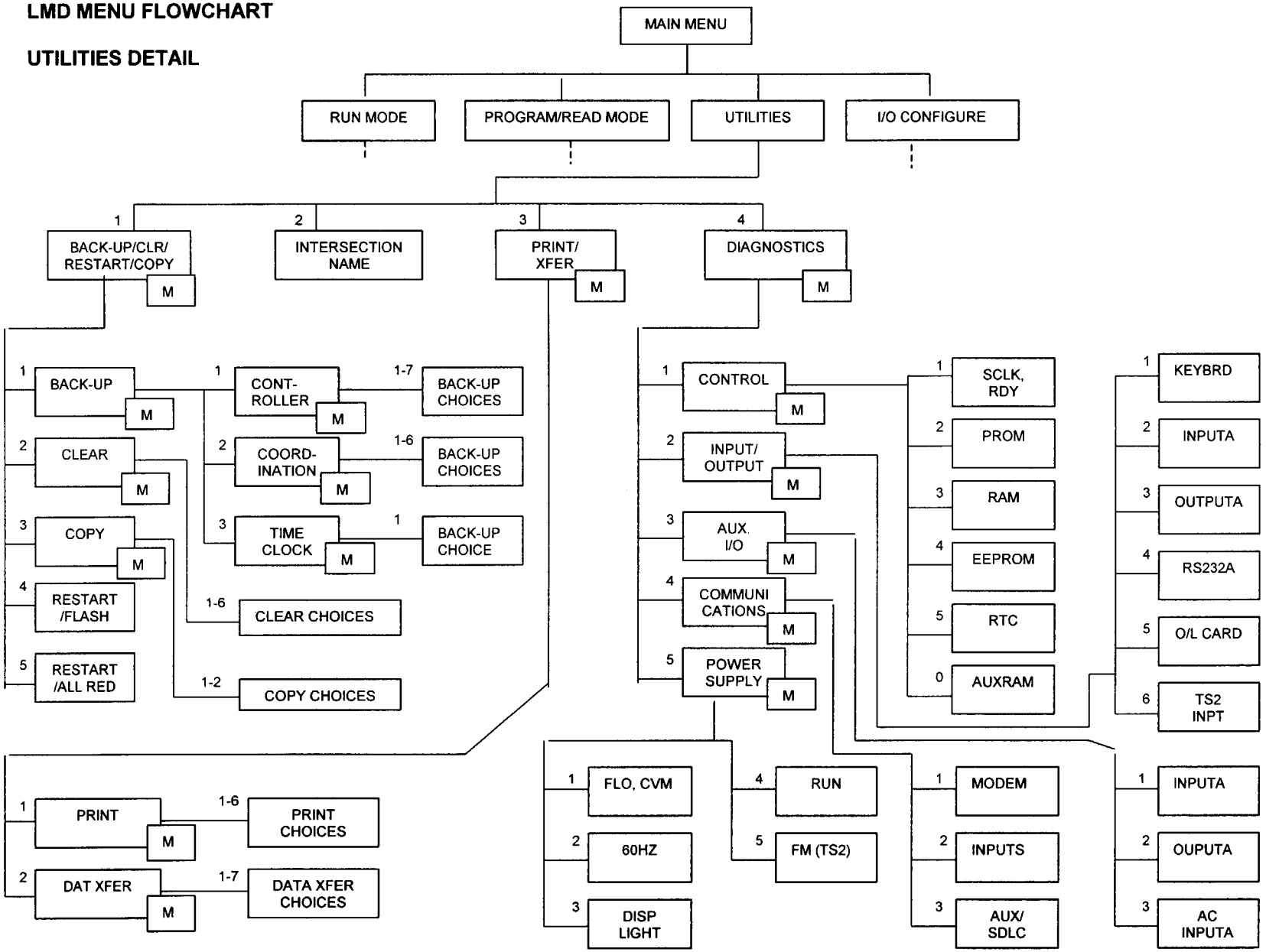
UTILITIES DETAIL



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I/O CONFIGURE DETAIL